Publications List of Prof. Shen-Li Chen

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◎ Professional Specialty

- Specialized in the VLSI Reliability, Power Electronics, and IC Design Areas.

A. Journal papers: (2010~2016)


27. Shen-Li Chen* and Dun-Ying Shu, "By Using Grey System and Fuzzy-Neural Network to Predict the Threshold Voltage of Complicated Sub-micron MOSFETs", *WIT Transactions on Engineering Sciences*, vol. 92, pp. 537-544, Jun. 2014.


B. Book Chapter Series: (2010~2016)


C. Conference Papers: (2010~2016)


4. Shen-Li Chen*, Yu-Ting Huang, Chih-Hung Yang, Kuei-Jyun Chen, Yi-Cih Wu, Jia-Ming Lin, Chih-Ying Yen, "ESD Reliability Improvement by the Source-Discrete Placement in a 45-V pLDMOS-SCR (npn-Type)," IEEE 6th International Conference on Power and Energy (PECON), Melaka, Malaysia, Nov. 2016. (accepted)


7. Shen-Li Chen*, Min-Hua Lee, and Tzung-Shian Wu, "Influences of Substrate Pickup Integrated with the Source-end Engineering on ESD/Latch-up Reliabilities in a 0.35-μm 3.3-V Process," IEEE International Symposium on Computer, Consumer


17. Shen-Li Chen*, Yu-Ting Huang, Chih-Hung Yang, Chih-Ying Yen, Kuei-Jyun Chen, Yi-Cih Wu, and Jia-Ming Lin, "Drain Side N+ Layout Manners ("npnnpn" Arranged-type) on ESD Robustness in the 60-V pLDMOS-SCR", 12th International Symposium on Measurement Technology and Intelligent Instruments, Taipei, Taiwan, Sep. 2015. (accepted)

18. Shen-Li Chen*, Dun-Ying Shu, "By Using Grey System and Neural-Fuzzy Network
Methods to obtain the Threshold Voltage of Submicron n-MOSFET DUTs", IEEE 12th International Conference on Fuzzy Systems and Knowledge Discovery (FSKD), pp. 501-505, Zhangjiajie, China, Aug. 2015.


29. Shen-Li Chen*, Yu-Ting Huang, Shawn Chang, Shun-Bao Chang, "Layout-Type Influences of Anti-ESD Ability in 60-V pLDMOS Power DUTs with the Embedded


50. Shen-Li Chen*, Yi-Sheng Lai, Min-Hua Lee, Chun-Ju Lin, "Influences of Source Pick-up Adding and ESD Implanted Layer for the ESD Robustness", 8th International Conference on Green Energy Technology and Management (GETM2013), Changhua, Taiwan, pp.7 ~ 10, Jun. 2013.

51. Shen-Li Chen*, Min-Hua Lee, Yi-Sheng Lai, Chun-Ju Lin, "Impact of n-Well and FOD Adding on the ESD Robustness in 0.35μm LV MOSTs”, 8th International Conference on Green Energy Technology and Management (GETM2013), Changhua, Taiwan, pp.1 ~ 6, Jun. 2013.

52. Shen-Li Chen*, Min-Hua Lee, Chun-Ju Lin, and Yi-Sheng Lai,"


54. Shen-Li Chen* and Min-Hua Lee, “Layout Strategy of P+ Pick-up on the LV MOST ESD Reliability in 0.6μm to 0.18μm CMOS Processes”, *IEEE International Symposium on Next-Generation Electronics*, Kaohsiung, Taiwan, pp.51～54, Feb. 2013.


nLDMOS”, IEEE International Symposium on Next-Generation Electronics, Kaohsiung, Taiwan, pp.182-185, Nov. 2010.


D. Patents 專利：(2010~2016)

1. 陳勝利，”高压半导体器件”， 中華人民共和國实用新型专利，證書# CN 4096403 (ZL2014-2-0484361.3), pp. 1~15, 2014.08.26~2023.08.25.
2. 陳勝利，”半导体结构”， 中華人民共和國实用新型专利，證書# CN 4085412 (ZL2014-2-0375327.2), pp. 1~11, 2014.07.08~2023.07.07
3. 陳勝利，”发光二极管”， 中華人民共和國实用新型专利，證書# CN 4050394 (ZL2014-2-0375246.2), pp. 1~11, 2014.07.08~2023.07.07
5. 陳勝利，”發光二極體”，中華民國新型專利，證書# TW M487526, pp. 16151-16157, Oct. 2014 (2014.10.01 ~ 2024.05.25).
7. 陳勝利，”具有可控硅整流器結構之高壓半導體元件”，中華民國新型專利，證書# TW M518408, pp. 14213-14217, 2016.03.01 ~ 2025.09.23.
8. 陳勝利，”抗靜電放電的高壓半導體元件”， 中華民國新型專利，TW M518409, pp. 14218-14220, 2016.03.01 ~ 2025.09.23.

E. Award 獎項：(2010~2016)

| 優等設計獎 | 黃郁婷，陳勝利 CIC 晶片設計競賽，民國 105 年 8 月 |