Publication List of Kuen-Wey Lin (林昆蔚)

International journal articles

1. K.-W. Lin, Y.-S. Lin, Y.-L. Li, and R.-B. Lin, “A maze routing-based methodology with bounded exploration and path-assessed retracing for constrained multi-layer obstacle-avoiding rectilinear Steiner tree construction,” *ACM Transactions on Design Automation of Electronic Systems*, 23, 4, Article 45, May 2018.

Domestic journal articles

1. 張永嘉、楊健生、林昆蔚(2022)。量子電腦之電路設計發展與應用。《電工通訊季刊》，2022年第3季(2022/09)，54－65。https://doi.org/10.6328/CIEE.202209_(3).0006.

Conference papers (Proceedings)

1. Y. -Y. Li and K. -W. Lin, " An Efficient Multi-Task Network for Real-Time Emotion and Gender Classification on Low-Resource Platforms," in *Proc. of the IEEE International Conference on Applied System Innovation (ICASI)*, Tokyo, Japan, 2024, pp. 13-15.
2. K. -W. Lin, Y. -Y. Li, K. -J. Wang and M. -C. Tung, "Deploying Pre-Quantized Deep Learning Models on Heterogeneous Platforms with Operator Flow Recognition and Quantization Parameter Optimization," in *Proc. of the IEEE International Conference on Applied System Innovation (ICASI)*, Chiba, Japan, 2023, pp. 77-79.
3. K.-W. Lin, M. Hashimoto, and Y.-L. Li, “Near-future traffic evaluation based navigation for automated driving vehicles considering traffic uncertainties,” in *Proc. of the IEEE International Symposium on Quality Electronic Design*, Santa Clara, CA, Mar. 13-14, 2018, pp. 425-431.
4. K.-W. Lin, Y.-L. Li, and M. Hashimoto, “Near-future traffic evaluation based navigation for automated driving vehicles,” in *Proc. of the IEEE Intelligent Vehicle Symposium*, Los Angeles, CA, June 11-14, 2017, pp. 1465-1470.
5. K.-W. Lin, Y.-S. Lin, Y.-L. Li, and R.-B. Lin, “A maze routing-based algorithm for ML-OARST with pre-selecting and re-building Steiner points,” in *Proc. of the ACM Great Lakes Symposium on VLSI*, Alberta, Canada, May 10-12, 2017, pp. 399- 402.
6. M.-Yi Lin, Y.-L. Li and K.-W. Lin, “Color balancing aware double patterning,” in *Proc. of the IEEE International Conference on Applied System Innovation*, Sapporo, Japan, May 13-17, 2017, pp. 284-287.

7. S. Saurabh, K.-W. Lin, and Y.-L. Li, “Cellular automata based hardware accelerator for parallel maze routing,” in *Proc. of the IEEE International Conference on Advanced Materials for Science and Engineering*, Tainan, Taiwan, Nov. 12-13, 2016, pp. 680-683.
8. K.-W. Lin, Y.-L. Li, and R.-B. Lin, “Multiple-patterning lithography-aware routing for standard cell layout synthesis,” in *Proc. of the IEEE Asia Pacific Conference on Circuits and Systems*, Jeju, South Korea, Oct. 25-28, 2016, pp. 534-537.
9. T.-K. Lin, K.-W. Lin, C.-H. Chiu, and R.-B. Lin, “Logic block and design methodology for via-configurable structured ASIC using dual supply voltages,” in *Proc. of the ACM Great Lakes Symposium on VLSI*, Houston, TX, May 21-23, 2014, pp. 111-116.
10. Y.-C. Chen, H.-Y. Pang, K.-W. Lin, R.-B. Lin, H.-H. Tung, and S.-C. Su, “Via configurable three-input lookup-tables for structured ASICs,” in *Proc. of the ACM Great Lakes Symposium on VLSI*, New York, NY, May 16-18, 2010, pp. 49-54.
11. S.-Y. Chen, R.-B. Lin, H.-H. Tung and K.-W. Lin, "Power gating design for standard-cell-like structured ASICs," in *Proc. of the ACM/EDAA/IEEE Design, Automation and Test in Europe*, Dresden, Germany, Mar. 8-12, 2010, pp. 514-519.

Patents

1. 林昆蔚、李順河、李彥瑩、董明智。神經網路模型的深度學習編譯方法及儲存對應程式之非暫態電腦可讀取媒體。中華民國發明專利 I870179，核准日 2025-01-11。