Publications List of Prof. Shen-Li Chen (陳勝利)

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Research Fields (Expertise):

- Power Electronics, BCD Process (HV, UHV)
- VLSI Reliability
- ESD/EOS Protection Design
- CMOS Latchup Free Design/Testing
- System EMC/EMS Testing and Troubleshooting

Relevant Certificates of Conformity (相關合格證照):

1. TAF 實驗室認證規範 ISO/IEC 17025 訓練合格
   (Certificate No.: TAF-QM110006-C-24)
2. TAF 測試實驗室主管訓練合格
   (Certificate No.: TAF-TH110008-C-05)
3. ESD S20.20 Induction and Practice 訓練合格
   (DNV.GL Certificate No.: 20.26.01P.011)
4. ESD S20.20: 2021 Induction Course 訓練合格
   (DNV.GL Certificate No.: 21.26.02P.007)
5. ESG 師資培訓與認證訓練合格
   (Certificate No.: TISDA-ESG-MM-20240152)

A. Referred Journal papers: (2015~2023)

1. Shen-Li Chen*, Wei-Jung Chen, Chih-Ying Yen, "Analyzing ESD Reliability Strengthening of 40-V nLDMOS with Drain-Side Parasitic SCRs," International Journal of Electrical, Electronics and Data Communication, vol. 11(9), pp. 6-11, Sep. 2023.
2. Xing Chen Mai, Shen-Li Chen*, Hung Wei Chen, Yi Mu Lee, "Impacts of Floating Poly on Electrostatic Discharge Protection of Power-managed High-voltage Laterally Diffused

Metal Oxide Semiconductor Components," Electronics, vol. 12(13), pp. 2803-1–2803-13, Jun. 2023.

3. Jhong-Yi Lai, Shen-Li Chen*, Zhi-Wei Liu, Hung-Wei Chen, Hsun-Hsiang Chen, and Yi-Mu Lee, "Electrostatic-discharge Reliability Sensing of Ultrahigh-voltage N-channel Lateral-diffused MOSFETs Modulated by Different Operating Voltages," Sensors and Materials, vol. 34, no.5, pp.1835-1844, May 2022.
4. Zhi-Wei Liu, Shen-Li Chen*, Jhong-Yi Lai, Hung-Wei Chen, Hsun-Hsiang Chen, and Yi-Mu Lee, "Electrostatic Discharge Sensing of Concentric Circles of Poly2 with Different Potentials and Discrete High-voltage P-well Modulation on Circular Ultrahigh-voltage N-channel Laterally Diffused MOSFET Devices," Sensors and Materials, vol. 34, no.5, pp.1823-1833, May 2022.
5. Shen-Li Chen*, Po-Lin Lin, Hung-Wei Chen, and Yi-Mu Lee, "High Reliabilities Design of Stacked Ultra-high-voltage nLDMOSs in a 0.5-μm BCD Semiconductor Technology," Modern Concepts in Material Science, vol. 4(5), pp. 593-1–593-6, Nov. 2021.
6. Shi-Zhe Hong, Shen-Li Chen*, Hung-Wei Chen, and Yi-Mu Lee, "Drain Side Area-modulation Effect of Parasitic Schottky Diode on ESD Reliability for High Voltage P-channel Lateral-Diffused MOSFETs," IEEE Electron Device Letters, vol. 42(10), pp. 1512-1515, Oct. 2021.
7. Tien-Yu Lan, Shen-Li Chen*, Hung-Wei Chen, and Yi-Mu Lee, "Research on ESD Protection of Ultra-high Voltage nLDMOS Devices by Super-junction Engineering in the Drain-side Drift Region," IEEE Journal of the Electron Devices Society, vol.9, pp. 763-777, Aug. 2021.
8. Shi-Zhe Hong and Shen-Li Chen*, "ESD Design and Analysis by Drain Electrode-embedded Horizontal Schottky Elements for HV nLDMOSs," Electronics, vol. 10(1), pp. 178-1–178-15, Jan. 2021.
9. Po-Lin Lin, Shen-Li Chen* and Sheng-Kai Fan, "Enhance the ESD Ability of UHV 300-V Circular LDMOS Components by Embedded SCRs and the Robustness P-body Well," IEEE Journal of the Electron Devices Society, vol.9, pp. 108-113, Jan. 2021.
10. Po-Lin Lin, Shen-Li Chen* and Sheng-Kai Fan, "ESD-Performance Enhancement of Circular Ultra-High-Voltage 300-V N-Channel Lateral-Diffused MOSFETs by Source/Drain Embedded Schottky Diodes," IEEE Electron Device Letters, vol. 41(11), pp. 1673-1676, Nov. 2020.
11. Hung-Wei Chen, Shen-Li Chen*, Yu-Ting Huang, and Hsun-Hsiang Chen, "ESD improvements on power N-channel LDMOS devices by the Composite Structure of super junctions integrated with SCRs in the drain side," IEEE Journal of the Electron Devices Society, vol.8, pp. 864-872, Jul. 2020.
12. Shen-Li Chen* and S.P. Lee, "Optimized Design of the 100-V Silicon Based Power N-channel LDMOS Transistor," Modern Concepts in Material Science, vol. 3(2), pp. 559-1–559-6, Jul. 2020.
13. Shen-Li Chen*, Pei-Lin Wu and Yu-Jen Chen, "Robust ESD-Reliability Design of 300-V Power N-channel LDMOSs with the Elliptical Cylinder Super-junctions in the Drain Side," Electronics, vol. 9(4), pp. 730-1–730-14, Apr. 2020.

14. Sheng-Kai Fan, Shen-Li Chen*, Po-Lin Lin, and Hung-Wei Chen, "Layout Strengthening the ESD Performance for High-voltage N-channel Lateral Diffused MOSFETs," Electronics, vol. 9(4), pp. 718-1–718-20, Apr. 2020.
15. Po-Lin Lin, Shen-Li Chen* and Sheng-Kai Fan, "ESD-Immunity Impacts in 300 V nLDMOS by Comprehensive Drift-region Engineering," Electronics, vol. 8(12), pp. 1469-1-1469-14, 2019.
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19. Shen-Li Chen*, Yu-Ting Huang, and Shawn Chang, "Design and Impact on ESD/LU Immunities by Drain-side Super-junction Structures in Low-(High-)Voltage MOSFETs for the Power Applications," IEICE Trans. on Electronics, vol. E101-C (3), pp. 141-150, Mar. 2018.
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23. Shen-Li Chen* and Shawn Chang, "Robust Reliability and Electrical Performances by the Bulk-Contact in 60-V p-channel LDMOS Power Components," International Journal of Green Energy, vol. 14(3), pp. 239-244, Mar. 2017.
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26. Shen-Li Chen* and Yu-Ting Huang, "Design and Layout Strategy in the 60-V Power pLDMOS with Drain-End Modulated Engineering of Reliability Considerations", IEEE Transactions on Power Electronics, vol. 31(7), pp.5113-5121, Jul. 2016.

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39. Shen-Li Chen*, Shawn Chang, Yu-Ting Huang, Shun-Bao Chang, "Reliability Enhancement in the 60 V Power pLDMOS by a Bulk-FOD Engineering," Advanced Materials Research, vols. 1079-1080, pp. 506-509, Jan. 2015.

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2. Shen-Li Chen*, Pei-Lin Wu and Yu-Jen Chen, "Robust ESD-Reliability Design of 300-V Power N-channel LDMOSs with the Elliptical Cylinder Super-junctions in the Drain Side," Industrial Applications of Power Electronics (ISBN: 978-3-03943-483-1), pp. 265-278, MDPI Publisher(Editor: Eduardo M. G. Rodrigues), Basel, Switzerland, Dec. 2020.
3. Po-Lin Lin, Shen-Li Chen* and Sheng-Kai Fan, "ESD-Immunity Impacts in 300 V nLDMOS by Comprehensive Drift-region Engineering," Intelligent Electronic Devices (ISBN: 978-3-03928-973-8), pp. 91-104, MDPI Publisher(Editor: Teen-Hang Meen), Basel, Switzerland, May 2020.
4. Shen-Li Chen*, Yi-Cih Wu, "Sensing and Reliability Improvement of Electrostatic-Discharge Transient by Discrete Engineering for High-Voltage 60-V N-Channel Lateral-Diffused MOSFETs with Embedded Silicon-Controlled Rectifiers," Top 5 Contributions on Sensor and Biosensor Technology, 2nd Edition (ISBN: 978-93-88170-19-2), pp. 2-22, AVID SCIENCE Publisher(Editor: Priyanka), Berlin, Germany, Dec. 2018.
5. Shen-Li Chen*, Chun-Ju Lin, and Yu-Ting Huang, "Impacts of ESD Reliability by Different Layout Engineering in the 0.25-μm 60-V High-voltage LDMOS Devices," Nano Devices and Sensors (ISBN 978-1-5015-1050-2), pp. 177-197, De Gruyter Publisher, Berlin, Germany, Mar. 2016.
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7. Shen-Li Chen*, Yu-Ting Huang, Shawn Chang, Shun-Bao Chang, “N+ Extended-Distribution Influences on Anti-ESD Ability in the 60-V pLDMOS-SCR (NPN arranged-type),” Lecture Notes in Electrical Engineering (ISBN: 978-3-319-17313-9), vol. 345, Chap. 74, pp.579-585, New York, USA, Springer publisher, Jan. 2016.

C. Referred Conference Papers: (2015~2024)

1. Xiu-Yuan Yang, Shen-Li Chen*, Ting-En Lin, Hung-Wei Chen, and Yi-Mu Lee, " ESD/Latch-up Immunities Enhancements of HV NLDMOSs by the Embedded Discrete SCR/Schottky Alternating Arrangement Design at the Drain Side," IEEE International Conference on Consumer Electronics (ICCE-TW), Taichung, Taiwan, Jul. 2024, pp. 783-784.
2. Ting-En Lin, Shen-Li Chen*, Xiu-Yuan Yang, Hung-Wei Chen, and Yi-Mu Lee, " Latchup-reliability Impact of High-Voltage nLDMOSs with the Parasitic Schottky Area Modulation in the Source Side," IEEE International Conference on Consumer Electronics (ICCE-TW), Taichung, Taiwan, Jul. 2024, pp. 791-792.
3. Xiu-Yuan Yang, Shen-Li Chen*, Ting-En Lin, Hung-Wei Chen, and Yi-Mu Lee, " ESD/Latch-Up Reliability Enhancements of HV nLDMOSs by Drain-End Horizontally Embedding Different Discrete P^+ SCRs," IEEE 10th International Conference on Applied

System Innovation, Kyoto, Japan, Apr. 2024, pp. 27-28.

4. Ting-En Lin, Shen-Li Chen*, Xiu-Yuan Yang, Hung-Wei Chen, and Yi-Mu Lee, " Study on Enhancing ESD Reliability through A Area Modulation of High-Voltage nLDMOSs with the Drain Embedded STI," IEEE 10th International Conference on Applied System Innovation, Kyoto, Japan, Apr. 2024, pp. 46-48.
5. 楊修源, 陳勝利*, 林廷恩, "高壓 nLDMOS 汲極端水平嵌入離散 P^+ SCR 之抗 ESD/栓鎖效應可靠度研究," 中國機械工程學會第四十屆全國學術研討會, Changhua, Taiwan, Dec. 2023, pp.927-929.
6. 林廷恩, 陳勝利*, 楊修源, "高壓 nLDMOS 汲極端嵌入 STI 面積調變對可靠度增強之研究," 中國機械工程學會第四十屆全國學術研討會, Changhua, Taiwan, Dec. 2023, pp.930-932.
7. 陳勛祥, 林家丞, 陳勝利, "10 位元 10MHz 取樣頻率之 CMOS 導管式類比數位轉換器設計," 中國機械工程學會第四十屆全國學術研討會, Changhua, Taiwan, Dec.. 2023, pp.933-935.
8. 林廷恩, 陳勝利*, 劉誌瑋, 楊修源, "高壓 nLDMOS 汲極端寄生 Schottky/SCR 面積調變之抗 ESD 能力探討," T-ESD & Reliability Conference, Hsinchu, Taiwan, Nov. 2023, pp.C3-1- C3-4.
9. Xiu-Yuan Yang, Shen-Li Chen*, Ting-En Lin, "高壓 nLDMOS 汲極端垂直嵌入 SCR 暨離散 P^+ SCR 之抗 ESD 能力研究," T-ESD & Reliability Conference, Hsinchu, Taiwan, Nov. 2023, pp.C2-1- C2-4.
10. Xiu-Yuan Yang, Shen-Li Chen*, Ting-En Lin, "ESD-Robustness Study of High-voltage nLDMOSs with Vertically Embedded SCR and Discrete P^+ SCR in the Drain Side," IEEE 5th Eurasia Conference on IoT, Communication and Engineering (ECICE), Yunlin, Taiwan, Oct. 2023, pp.193-196.
11. Ting-En Lin, Shen-Li Chen*, Zhi-Wei Liu, Xiu-Yuan Yang, "Impacts of Embedded SCR/Schottky Parasitics on ESD Reliability in the Drain Side of High Voltage nLDMOS Devices," IEEE 5th Eurasia Conference on IoT, Communication and Engineering (ECICE), Yunlin, Taiwan, Oct. 2023, pp.208-211.
12. Shen-Li Chen*, Wei-Jung Chen, Chih-Ying Yen, "Analyzing ESD Reliability Strengthening of 40-V nLDMOS with Drain-Side Parasitic SCRs," 1616th International Conference on Recent Innovations in Engineering and Technology (1616th ICRIET), Zurich, Switzerland, Aug. 2023, pp. 39-44.
13. Xiu-Yuan Yang, Shen-Li Chen*, Jhong-Yi Lai, Xing-Chen Mai, Yu-Jie Chung, and Ting-En Lin, "ESD-capability Study of High-voltage nLDMOSs with the Drift Region DPW Engineering," IEEE International Conference on Consumer Electronics (ICCE-TW), Pingtung, Taiwan, Jul. 2023, pp.223-224.
14. Ting-En Lin, Shen-Li Chen*, Zhi-Wei Liu, Xing-Chen Mai, Xiu-Yuan Yang, and Yu-Jie Chung, "High-voltage nLDMOS Drain Side Schottky/SCR Modulations for Enhancement Reliability Capabilities," IEEE International Conference on Consumer Electronics (ICCE-TW), Pingtung, Taiwan, Jul. 2023, pp.225-226.
15. Xing-Chen Mai, Shen-Li Chen*, Jhong-Yi Lai, Zhi-Wei Liu, and Yu-Jie Chung, "ESD-capability Impacts of the Resurf NBL Length on High-voltage nLDMOSs," 9th IEEE International Conference on Applied System Innovation (ICASI), Tokyo, Japan, Apr. 2023, pp.65-67.
16. Yu-Jie Chung, Shen-Li Chen*, Xing-Chen Mai, Ting-En Lin, and Xiu-Yuan Yang,"

Robust ESD Capability of High-voltage nLDMOSs with Embedded Floating P+ Structures in the Drain Side," 9th IEEE International Conference on Applied System Innovation (ICASI), Tokyo, Japan, Apr. 2023, pp.74-76.

17. Jhong-Yi Lai, Wei-Jung Chen, Shen-Li Chen*, "Enhanced ESD-capability of High-voltage 32 V N-Channel LDMOSs with the Body-side Hetero-junction Structure," 13th International Conference on Power, Energy and Electrical Engineering, Tokyo, Japan, Feb. 2023, pp.17-21.
18. 鍾宇傑, 陳勝利*, 麥新承, 林廷恩, 楊修源, "汲極端寄生蕭特基二極體/加入 STI 結構對高壓 nLDMOS 抗 ESD 能力之探討," 第十九屆台灣電力電子研討會, Taichung, Taiwan, Dec. 2022, pp.004-1- 004-4.
19. 麥新承, 陳勝利*, 鍾宇傑, 楊修源, 林廷恩, "高壓 nLDMOS 在汲極側漂移區設計不同 RESURF 結構之抗 ESD 能力影響研究," 第十九屆台灣電力電子研討會, Taichung, Taiwan, Dec. 2022, pp.002-1- 002-4.
20. Yu-Jie Chung, Shen-Li Chen*, Zhi-Wei Liu, Jhong-Yi Lai and Xing-Chen Mai, "汲極端寄生蕭特基元件/矽控整流器並嵌入 HVPB 結構對高壓 nLDMOS 抗 ESD 能力影響之探討", T-ESD & Reliability Conference, Hsinchu, Taiwan, Nov. 2022, pp.B1-1- B1-5.
21. Xing-chen Mai, Shen-Li Chen*, Yu-Jie Chung, Xiu-Yuan Yang and Ting-En Lin, "高壓 nLDMOS 三電極區寄生蕭特基二極體之 ESD 可靠度能力探討", T-ESD & Reliability Conference, Hsinchu, Taiwan, Nov. 2022, pp.B2-1- B2-6.
22. Xing-Chen Mai, Shen-Li Chen*, Xiu-Yuan Yang, Ting-En Lin, and Yu-Jie Chung, " ESD-immunity Impacts of High-voltage nLDMOS with RESURF Structures in the Drain-side Drift Region", International Conference on Machining, Materials and Mechanical Technologies (IC3MT), Taipei, Taiwan, Nov. 2022. (accepted)
23. Yu-Jie Chung, Shen-Li Chen*, Xing-Chen Mai, Xiu-Yuan Yang, and Ting-En Lin, "Robust ESD Ability of High Voltage nLDMOSs with Drain-side Adding Schottky/STI", International Conference on Machining, Materials and Mechanical Technologies (IC3MT), Taipei, Taiwan, Nov. 2022. (accepted)
24. Xing-Chen Mai , Shen-Li Chen*, Yu-Jie Chung, Xiu-Yuan Yang, and Ting-En Lin, "Study of the Turns Impact on ESD-immunity of High-voltage nLDMOSs with a Constant Floating-poly Area", IEEE 4th International Conference of Eurasia Conference on IOT, Communication and Engineering (ECICE), Yunlin, Taiwan, Oct. 2022, pp.176-178.
25. Yu-Jie Chung, Shen-Li Chen*, Zhi-Wei Liu, Jhong-Yi Lai and Xing-Chen Mai, " ESD-ability Analysis of High Voltage nLDMOSs with the Drain-side Parasitic Schottky/Embedded Shallow-trench Isolation", IEEE 4th International Conference of Eurasia Conference on IOT, Communication and Engineering (ECICE), Yunlin, Taiwan, Oct. 2022, pp. 151-153.
26. Hsun-Hsiang Chen, You Zhang, Shen-Li Chen, "A Study of ESD Reliability on Gate and Drain to Source and Substrate Stress by Structure Modulation in 0.18 μm 6 V nLDMOS Devices", IET International Conference on Engineering Technologies and Applications (IET ICETA), Changhua, Taiwan, Oct. 2022, pp. 1-2.
27. Xing-Chen Mai, Shen-Li Chen*, Jhong-Yi Lai, Zhi-Wei Liu, and Yu-Jie Chung, " ESD-immunity Study of High-voltage nLDMOS with Vertical Parasitic Schottky Structures in the Source End," IET International Conference on Engineering

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28. Yu-Jie Chung, Shen-Li Chen*, Zhi-Wei Liu, Jhong-Yi Lai, and Xing-Chen Mai, " ESD-ability Enhancement of High Voltage pLDMOSs with the Discrete Source Side," IET International Conference on Engineering Technologies and Applications (IET ICETA), Changhua, Taiwan, Oct. 2022, pp. 1-2.
29. Xing-Chen Mai, Shen-Li Chen*, Jhong-Yi Lai, Zhi-Wei Liu, and Yu-Jie Chung, " ESD-robustness Enhancement of High-voltage Octagonal nLDMOSs with an Embedded Schottky Diode Modulation in the Bulk Electrode," The 5th NIT-NUU Bilateral Academic Conference, Miaoli, Taiwan, Sep. 5, 2022, pp.1-2.
30. Yu-Jie Chung, Shen-Li Chen*, Zhi-Wei Liu, Jhong-Yi Lai, and Xing-Chen Mai, " Robust ESD Capability Design of High Voltage nLDMOSs with the Drain-side Parasitic SCR Structures by TCAD Simulation," The 5th NIT-NUU Bilateral Academic Conference, Miaoli, Taiwan, Sep. 5, 2022, pp.1-2.
31. Zhi-Wei Liu, Shen-Li Chen*, Jhong-Yi Lai, Xing-Chen Mai, and Yu-Jie Chung, "An Investigation of ESD-Enhancement by the Drain-side Embedded SCR Area Modulation for HV pLDMOSs," IEEE International Conference on Consumer Electronics (ICCE-TW), Taipei, Taiwan, Jul. 2022, pp.73-74.
32. Jhong-Yi Lai, Shen-Li Chen*, Zhi-Wei Liu, Xing-Chen Mai and Yu-Jie Chung, "ESD Capability Analysis of High-voltage nLDMOSs by the Bulk Terminal Modulation," IEEE International Conference on Consumer Electronics (ICCE-TW), Taipei, Taiwan, Jul. 2022, pp. 71-72.
33. Shen-Li Chen* and Po-Lin Lin, "Holding-voltage Enhancement of Power Management Silicon Based UHV 300-V Circular LDMOS Components by Source Side Engineering," Advances in Functional Materials (AFM) Conference, Kyushu, Japan, July 2022. (accepted)
34. 鍾宇傑，陳勝利*，劉誌瑋，賴忠義，麥新承，"汲極端寄生矽控整流器結構對高壓 nLDMOS 抗 ESD 能力探討," 第十六屆智慧生活科技研討會(ILT2022), Taichung, Taiwan, Jun 2022, pp.239-242.
35. 麥新承，陳勝利*，劉誌瑋，賴忠義，鍾宇傑，"汲極端寄生蕭特基二極體結構調變對於高壓 LDMOS 抗 ESD 能力之探討," 第十六屆智慧生活科技研討會(ILT2022), Taichung, Taiwan, Jun 2022, pp.229-232.
36. Zhi-Wei Liu, Shen-Li Chen* and Jhong-Yi Lai, "ESD Study of HV 65V nLDMOSs with the Drain-side Parasitic SCR Modulation," International Electrostatic Discharge Virtual Workshop(IEW), Hsinchu, Taiwan, May 3-6, 2022, pp.1-6.
37. Jhong-Yi Lai, Shen-Li Chen* and Zhi-Wei Liu, "An ESD Investigation of 100V UHV nLDMOSs Embedded with the Schottky/SCR in the Drain End," International Electrostatic Discharge Virtual Workshop(IEW), Hsinchu, Taiwan, May 3-6, 2022, pp.1-6.
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