

# **Publications List of Prof. Shen-Li Chen**

**Phone: +886-37382525 (O)**

**Dept. of Electronic Engineering, National United U.**

**2 Lien-Da Rd., MiaoLi City 36063, Taiwan**

**EMail: jackchen@nuu.edu.tw**

**jackchen2100@gmail.com**

## **Research Fields (Expertise):**

- Power Electronics, BCD Process (HV, UHV)
- VLSI Reliability
- ESD/EOS Protection Design
- CMOS Latchup Free Design/Testing
- System EMC/EMS Testing and Troubleshooting

## **Relevant Certificates of Conformity (相關合格證照):**

1. ESD S20.20 Induction and Practice 訓練合格  
(DNV.GL Certificate No.: 20.26.01P.011)
2. ESD S20.20: 2021 Induction Course 訓練合格  
(DNV.GL Certificate No.: 21.26.02P.007)
3. TAF 實驗室認證規範 ISO/IEC 17025 訓練合格  
(Certificate No.: TAF-QM110006-C-24)
4. TAF 測試實驗室主管訓練合格  
(Certificate No.: TAF-TH110008-C-05)
5. ESG 師資培訓與認證訓練合格  
(Certificate No.: TISDA-ESG-JM-20240063)

## **Publication Papers & Projects (近年發表之論文與研究計劃):**

### **A. Referred Journal papers: (2014~2023)**

1. Xing Chen Mai, Shen-Li Chen\*, Hung Wei Chen, Yi Mu Lee, "Impacts of Floating Poly on ESD Protection of Power-managed High-voltage LDMOS Components," [Electronics](#), vol. 12(13), pp. 2803-1–2803-13, Jun. 2023.

2. Jhong-Yi Lai, Shen-Li Chen\*, Zhi-Wei Liu, Hung-Wei Chen, Hsun-Hsiang Chen, and Yi-Mu Lee, "Electrostatic-discharge Reliability Sensing of Ultrahigh-voltage N-channel Lateral-diffused MOSFETs Modulated by Different Operating Voltages," [Sensors and Materials](#), vol. 34, no.5, pp.1835-1844, 2022.
3. Zhi-Wei Liu, Shen-Li Chen\*, Jhong-Yi Lai, Hung-Wei Chen, Hsun-Hsiang Chen, and Yi-Mu Lee, "Electrostatic Discharge Sensing of Concentric Circles of Poly2 with Different Potentials and Discrete High-voltage P-well Modulation on Circular Ultrahigh-voltage N-channel Laterally Diffused MOSFET Devices," [Sensors and Materials](#), vol. 34, no.5, pp.1823-1833, 2022.
4. Shen-Li Chen\*, Po-Lin Lin, Hung-Wei Chen, and Yi-Mu Lee, "High Reliabilities Design of Stacked Ultra-high-voltage nLDMOSs in a 0.5- $\mu$ m BCD Semiconductor Technology," [Modern Concepts in Material Science](#), vol. 4(5), pp. 593-1–593-6, Nov. 2021.
5. Shi-Zhe Hong, Shen-Li Chen\*, Hung-Wei Chen, and Yi-Mu Lee, "Drain Side Area-modulation Effect of Parasitic Schottky Diode on ESD Reliability for High Voltage P-channel Lateral-Diffused MOSFETs," [IEEE Electron Device Letters](#), vol. 42(10), pp. 1512-1515, Oct. 2021.
6. Tien-Yu Lan, Shen-Li Chen\*, Hung-Wei Chen, and Yi-Mu Lee, "Research on ESD Protection of Ultra-high Voltage nLDMOS Devices by Super-junction Engineering in the Drain-side Drift Region," [IEEE Journal of the Electron Devices Society](#), vol.9, pp. 763-777, Aug. 2021.
7. Shi-Zhe Hong and Shen-Li Chen\*, "ESD Design and Analysis by Drain Electrode-embedded Horizontal Schottky Elements for HV nLDMOSs," [Electronics](#), vol. 10(1), pp. 178-1–178-15, Jan. 2021.
8. Po-Lin Lin, Shen-Li Chen\* and Sheng-Kai Fan, "Enhance the ESD Ability of UHV 300-V Circular LDMOS Components by Embedded SCRs and the Robustness P-body Well," [IEEE Journal of the Electron Devices Society](#), vol.9, pp. 108-113, Jan. 2021.
9. Po-Lin Lin, Shen-Li Chen\* and Sheng-Kai Fan, "ESD-Performance Enhancement of Circular Ultra-High-Voltage 300-V N-Channel Lateral-Diffused MOSFETs by Source/Drain Embedded Schottky Diodes," [IEEE Electron Device Letters](#), vol. 41(11), pp. 1673-1676, Nov. 2020.
10. Hung-Wei Chen, Shen-Li Chen\*, Yu-Ting Huang, and Hsun-Hsiang Chen, "ESD improvements on power N-channel LDMOS devices by the Composite Structure of super junctions integrated with SCRs in the drain side," [IEEE Journal of the Electron Devices Society](#), vol.8, pp. 864-872, Jul. 2020.
11. Shen-Li Chen\* and S.P. Lee, "Optimized Design of the 100-V Silicon Based Power N-channel LDMOS Transistor," [Modern Concepts in Material Science](#), vol. 3(2), pp. 559-1–559-6, Jul. 2020.
12. Shen-Li Chen\*, Pei-Lin Wu and Yu-Jen Chen, "Robust ESD-Reliability Design of 300-V Power N-channel LDMOSs with the Elliptical Cylinder Super-junctions in the Drain Side," [Electronics](#), vol. 9(4), pp. 730-1–730-14, Apr. 2020.

13. Sheng-Kai Fan, Shen-Li Chen\*, Po-Lin Lin, and Hung-Wei Chen, "Layout Strengthening the ESD Performance for High-voltage N-channel Lateral Diffused MOSFETs," [Electronics](#), vol. 9(4), pp. 718-1–718-20, Apr. 2020.
14. Po-Lin Lin, Shen-Li Chen\* and Sheng-Kai Fan, "ESD-Immunity Impacts in 300 V nLDMOS by Comprehensive Drift-region Engineering," [Electronics](#), vol. 8(12), pp. 1469-1-1469-14, 2019.
15. Shen-Li Chen\*, Pei-Lin Wu, Yu-Lin Jhou, Po-Lin Lin and Sheng-Kai Fan, "ESD-Protection Design of UHV Circular N-channel LDMOSs by the Drift Region with Elliptical Cylinder Super-junctions," [Advances in Technology Innovation](#), Dev. 2019 (accepted).
16. Shen-Li Chen\*, Pei-Lin Wu and Po-Lin Lin, "ESD-Reliability Enhancement of Circular UHV 300-V Power nLDMOSs by the Drain-side Superjunction Structure," [IEEE Electron Device Letters](#), vol. 40(4), pp. 597-600, Apr. 2019.
17. Shen-Li Chen\*, Yi-Cih Wu, "Sensing and Reliability Improvement of Electrostatic-Discharge Transient by Discrete Engineering for High-Voltage 60-V N-Channel Lateral-Diffused MOSFETs with Embedded Silicon-Controlled Rectifiers," [Sensors](#), vol. 18(10), pp. 3340-1-3340-10, Oct. 2018.
18. Shen-Li Chen\*, Yu-Ting Huang, and Shawn Chang, "Design and Impact on ESD/LU Immunities by Drain-side Super-junction Structures in Low-(High-)Voltage MOSFETs for the Power Applications," [IEICE Trans. on Electronics](#), vol. E101-C (3), pp. 141-150, Mar. 2018.
19. Shen-Li Chen\*, Chun-Ju Lin, and Yu-Ting Huang, "Impacts of ESD Reliability by Different Layout Engineering in the 0.25- $\mu$ m 60-V High-voltage LDMOS Devices," [Physical Sciences Reviews](#), vol.3, issue 2, pp. 1-15, Feb. 2018.
20. Shen-Li Chen\*, Yu-Ting Huang, and Yi-Cih Wu, "Design of High-ESD Reliability in HV Power pLDMOS Transistors by the Drain-side Isolated SCRs," [IEICE Trans. on Electronics](#), vol. E100-C (5), pp. 446-452, May 2017.
21. Shen-Li Chen\* and Min-Hua Lee, "Impacts of Leakage-Biasing Failure-mode Identification in the Transmission-Line Pulse Testing for Low-voltage/High-voltage MOSFET Components," [IEEE Transactions on Industry Applications](#), vol. 53(3), pp.2888-2893, Mar. 2017.
22. Shen-Li Chen\* and Shawn Chang, "Robust Reliability and Electrical Performances by the Bulk-Contact in 60-V p-channel LDMOS Power Components," [International Journal of Green Energy](#), vol. 14(3), pp. 239-244, Mar. 2017.
23. Shen-Li Chen\* and Dun-Ying Shu, "Measurement Forecast of Anomalous Threshold Voltages in BCD LV Submicron n-MOSFETs with Two Artificial Intelligence Methods", [Measurement](#), vol. 100, pp. 93-98, Mar. 2017.
24. Shen-Li Chen\*, Kuei-Jyun Chen, H.-W. Chen, "ESD Protection Design and Enhancement in the Power 60-V N-channel LDMOS by Embedded-SCR Anode Islands," [Electronics Letters](#), vol. 52(19), pp. 1639-1640, Sep. 2016.
25. Shen-Li Chen\* and Yu-Ting Huang, "Design and Layout Strategy in the 60-V Power pLDMOS with Drain-End Modulated Engineering of Reliability Considerations", [IEEE Transactions on Power Electronics](#), vol. 31(7), pp.5113-5121, Jul. 2016.

26. Hung-Wei Chen, Yi- Mu Lee, and Shen-Li Chen, "The Taste Sensors with Conductivity Measurement," [The Open Materials Science Journal](#), vol. 10, pp. 37-43, 2016.
27. Yeong-Lin Lai, Edward Y. Chang, Shen-Li Chen, K. B. Wang, Chun-Yi Zheng and Wen-Jung Chiang, "Characteristics of GaAs Power MESFETs with Double Silicon Ion Implantations for Wireless Communication Applications," [The Open Materials Science Journal](#), vol. 10, pp. 29-36, 2016.
28. Shen-Li Chen\*, Chin-Chai Chen, Yeong-Lin Lai, Wen-Jung Chiang and Hung-Wei Chen, "PL Intensity and Life-time Enhancements of the n-GaN Light-Emitting Diode During the Device Fabrication," [The Open Materials Science Journal](#), vol. 10, pp. 20-28, 2016.
29. Shen-Li Chen\*, "Editorial: Advanced Microelectronic and Nanoscale Semiconductor Materials & Applications," [The Open Materials Science Journal](#), vol. 10, pp. 18-19, 2016.
30. Shen-Li Chen\* and Min-Hua Lee, "ESD-Reliability Influences of an HV nLDMOS with Different Embedded SCR Structures in the Drain Side", [International Journal of Electrical and Electronics Engineering Research](#), vol. 6 (2), pp. 37-44, Apr. 2016.
31. Shen-Li Chen\* and Min-Hua Lee, "Reliability Analysis of P<sup>+</sup> Pickup on Anti-ESD Performance in Four CMOS Low-voltage Technology Nodes," [IETE Journal of Research](#), vol. 62(6), pp. 752-761, Apr. 2016.
32. Shen-Li Chen\* and Yu-Ting Huang, "Design of Reliability Improvement in HV p-channel LDMOS DUTs by a 0.25  $\mu$ m 60-V BCD Process", [International Journal of Electronics and Electrical Engineering](#), vol. 4 (3), pp. 210-214, Mar. 2016.
33. Shen-Li Chen\*, Min-Hua Lee, and Chun-Ju Lin, "Protection Design of the SCR Cooperation on ESD Reliability Performance in Microelectronics of Low-voltage/High-voltage N-channel MOSFET Devices," [Wulfenia \(Journal\)](#), vol. 22 (12-pt.2), pp. 7-21, Dec. 2015.
34. Shen-Li Chen\* and Yi-Sheng Lai, "Strengthen Anti-ESD Characteristics in an HV LDMOS with Super-Junction Structures," [IEEE Transactions on Power Electronics](#), vol. 30 (5), pp. 2375-2382, May 2015.
35. Shen-Li Chen\*, "The I-V Characteristic Prediction of BCD LV pMOSFET Devices Based on an ANFIS-Based Methodology", [Advances in Fuzzy Systems](#), vol. 2015, pp. 824524-1 ~ 824524-8, Feb. 2015.
36. Shen-Li Chen\*, Shawn Chang, Chun-Hsing Shih, Hsun-Hsiang Chen, "ESD-Reliability Analysis and Strategy of the GaN-based Light-Emitting Diodes", [Key Engineering Materials](#), vols. 656-657, pp. 57-62, May 2015.
37. Shen-Li Chen\*, Tsung-Shiung Lee, Yu-Ting Huang, "Impacts of MOS Device Characteristic Under Different Oxygen-Dose Participations in the Silicon Substrate", [Key Engineering Materials](#), vols. 656-657, pp. 8-13, May 2015.
38. Shen-Li Chen\*, Shawn Chang, Yu-Ting Huang, Shun-Bao Chang, "Reliability Enhancement in the 60 V Power pLDMOS by a Bulk-FOD Engineering," [Advanced Materials Research](#), vols. 1079-1080, pp. 506-509, Jan. 2015.

39. Shen-Li Chen\* and Hung-Wei Chen, "Pseudo-Failure Impacts on ESD Robustness in Integrated Circuits I/O Ports by the Parasitic Capacitance", [The Open Electrical and Electronic Engineering Journal](#), vol. 8, pp. 143-251, Dec. 2014..
40. Shen-Li Chen\*, "Enhanced Electrostatic Discharge Reliability in GaN-Based Light-Emitting Diodes by the Electrode Engineering", [IEEE/OSA Journal of Display Technology](#), vol. 10, no.10, pp. 779-785, Oct. 2014.
41. Shen-Li Chen\* and Chun-Ju Lin, "Layout Structure Dependence of 60-V nLDMOS Devices in the Anti-ESD Reliability Consideration", [Journal of Electrical and Control Engineering](#), vol. 4(5), pp. 1-9, Oct. 2014.
42. Shen-Li Chen\* and Shih-Hua Hsu, "Design of a High Performance Green-Mode PWM Controller IC with Smart Sensing Protection Circuits," [Sensors and Transducers Journal](#), vol. 176, issue 8, pp. 210-218, Aug. 2014.
43. Shen-Li Chen\* and Min-Hua Lee, "A Comprehensive Evaluation of Drain-side Layout Topologies on the Power nLDMOS ESD/LU Reliabilities," [Research Journal of Applied Sciences, Engineering and Technology](#), vol. 8(4), pp. 496-502, Jul. 2014.
44. Shen-Li Chen\* and Yi-Sheng Lai, "Anti-ESD Improvement of a Power nLDMOS with a Perpendicular Super-junction Construction in the Drain Side", [Applied Mechanics and Materials](#), Vol. 595, pp. 195-200, Jun. 2014.
45. Shen-Li Chen\*, Wen-Ming Lee and Chi-Ling Chu, "ESD Failure Analysis and Robustness Design in Vertical-Diffused MOS Transistors", [Advanced Materials Research](#), Vols. 926-930, pp.456-461, Jun. 2014.
46. Shen-Li Chen\*, Wen-Ming Lee, Chi-Ling Chu, "EMMI Failure-Distributed Analysis of ESD Zapping and Protection Designs in Power VDMOS ICs", [International Journal of Energy Science](#), vol.4, issue 3, pp. 77-84, Jun. 2014.
47. Shen-Li Chen\* and Dun-Ying Shu, "By Using Grey System and Fuzzy-Neural Network to Predict the Threshold Voltage of Complicated Sub-micron MOSFETs", [WIT Transactions on Engineering Sciences](#), vol. 92, pp. 537-544, Jun. 2014.
48. Shen-Li Chen\*, Wen-Ming Lee and Chi-Ling Chu, "ESD Hazard Analysis of VDMOS Power Components by Photoemission Spectroscopy", [WIT Transactions on Information and Communication Technologies](#), vol. 56, pp. 721-728, May 2014.
49. Shen-Li Chen\* and Min-Hua Lee, "Highly ESD Reliable HV Power nLDMOS Device with the Bulk FODs Design Technique", [Energy Education Science and Technology, Part A: Energy Science and Research](#), vol. 32 (5), pp.3115-3124, May 2014.
50. Shen-Li Chen\* and Min-Hua Lee, "ESD Reliability Improvement of an HV nLDMOS by the Bulk FODs Engineering", [AASRI Procedia -Journal- Elsevier](#), USA, vol. 7, pp. 114-119, May 2014.
51. Shen-Li Chen\* and Min-Hua Lee, "Impacts of the Drain-side nWell Adding on ESD Robustness in 0.25- $\mu$ m LV/HV nMOSTs", [AASRI Procedia -Journal- Elsevier](#), USA, vol. 7, pp. 51-56, May 2014.
52. Shen-Li Chen\*, Min-Hua Lee, "Drain Side nWell Influences on the Reliability Immunity of 0.25- $\mu$ m LV/HV GGnMOS Devices by TLP Testing and EDA Simulation", [WIT Transactions on Modelling and Simulation](#), vol. 60, pp. 1181-1185, Apr. 2014.

53. Shen-Li Chen\*, Der-Ann Fran, "Improvement on ESD Protection of Output Driver in DC Brushless Fan ICs by the FOD Protection Block", [Advanced Materials Research](#), Vols. 850-851, pp.449-453, Mar. 2014.
54. Shen-Li Chen\*, Min-Hua Lee, "Impact of Drain-side nWell Engineering on ESD Robustness in 0.35  $\mu\text{m}$  LV MOSTs", [Advanced Materials Research](#), Vols. 850-851, pp.7-11, Mar. 2014.
55. Shen-Li Chen\* and Yang-Shiung Cheng, "Signal Sensing by the Architecture of Embedded I/O Pad Circuits", [International Journal on Smart Sensing and Intelligent Systems](#), vol. 7, no. 1, pp.196-213, Mar. 2014.
56. Shen-Li Chen\*, Min-Hua Lee, "A Novel ESD/LU Protection Structure with Drain FODs for High-voltage nLDMOS Applications", [WIT Transactions on Information and Communication Technologies](#), vol. 49, pp. 533-540, Feb. 2014.
57. Shen-Li Chen\*, Chun-Ju Lin, "Layout-type Dependence on ESD/LU Immunities for LVTnSCR Devices in LV Applications", [WIT Transactions on Information and Communication Technologies](#), vol. 49, pp. 525-532, Feb. 2014.
58. Shen-Li Chen\* and Der-Ann Fran, "Implementation of ESD Protection for Output Driver ICs with SCR Circuits Techniques", [Applied Mechanics and Materials](#), vol. 464, pp.139-144, Feb. 2014.
59. Shen-Li Chen\*, Yi-Sheng Lai, "Effects of Source Pick-up Adding and ESD Implanted Layer on ESD Reliability of LV GGnMOSTs", [WIT Transactions on Engineering Sciences](#), vol. 87, pp. 175-182, Jan. 2014.
60. Shen-Li Chen\*, Min-Hua Lee, "The Pick-up Strategy of Multi-finger GDpMOSTs on ESD Robustness in a 0.35  $\mu\text{m}$  Process Technology", [WIT Transactions on Engineering Sciences](#), vol. 87, pp. 165-173, Jan. 2014.
61. Shen-Li Chen\*, Min-Hua Lee, "Impact of FODs Adding on the ESD/LU Reliabilities in 0.35  $\mu\text{m}$  3.3 V LV nMOSTs", [WIT Transactions on Engineering Sciences](#), vol. 87, pp. 155-163, Jan. 2014.

## B. Book Chapter Series: (2014~2023)

1. Shen-Li Chen\*, "The I-V Characteristic Prediction of BCD LV pMOSFET Devices based on an ANFIS-Based Methodology," [Prime Archives in Electronics](#), (ISBN: 978-93-90014-22-4), pp.1-20, Hyderabad, India, Jan. 2021.
2. Shen-Li Chen\*, Pei-Lin Wu and Yu-Jen Chen, "Robust ESD-Reliability Design of 300-V Power N-channel LDMOSs with the Elliptical Cylinder Super-junctions in the Drain Side," [Industrial Applications of Power Electronics](#) (ISBN: 978-3-03943-483-1), pp. 265-278, MDPI Publisher(Editor: Eduardo M. G. Rodrigues), Basel, Switzerland, Dec. 2020.
3. Po-Lin Lin, Shen-Li Chen\* and Sheng-Kai Fan, "ESD-Immunity Impacts in 300 V nLDMOS by Comprehensive Drift-region Engineering," [Intelligent Electronic Devices](#) (ISBN: 978-3-03928-973-8), pp. 91-104, MDPI Publisher(Editor: Teen-Hang Meen), Basel, Switzerland, May 2020.



4. Shen-Li Chen\*, Yi-Cih Wu, "Sensing and Reliability Improvement of Electrostatic-Discharge Transient by Discrete Engineering for High-Voltage 60-V N-Channel Lateral-Diffused MOSFETs with Embedded Silicon-Controlled Rectifiers," [Top 5 Contributions on Sensor and Biosensor Technology](#), 2nd Edition (ISBN: 978-93-88170-19-2), pp. 2-22, AVID SCIENCE Publisher(Editor: Priyanka), Berlin, Germany, Dec. 2018.
5. Shen-Li Chen\*, Chun-Ju Lin, and Yu-Ting Huang, "Impacts of ESD Reliability by Different Layout Engineering in the 0.25- $\mu$ m 60-V High-voltage LDMOS Devices," [Nano Devices and Sensors](#) (ISBN 978-1-5015-1050-2), pp. 177-197, De Gruyter Publisher, Berlin, Germany, Mar. 2016.
6. Shen-Li Chen\*, Shawn Chang, Yu-Ting Huang, Shun-Bao Chang, "Anti-ESD Improvement by the Bulk-FOX Structure in HV nLDMOS Devices," [Lecture Notes in Electrical Engineering](#) (ISBN: 978-3-319-17313-9), vol. 345, Chap. 73, pp.571-577, New York, USA, Springer publisher, Jan. 2016.
7. Shen-Li Chen\*, Yu-Ting Huang, Shawn Chang, Shun-Bao Chang, "N+ Extended-Distribution Influences on Anti-ESD Ability in the 60-V pLDMOS-SCR (NPN arranged-type)," [Lecture Notes in Electrical Engineering](#) (ISBN: 978-3-319-17313-9), vol. 345, Chap. 74, pp.579-585, New York, USA, Springer publisher, Jan. 2016.
8. Shen-Li Chen\*, Min-Hua Lee, Chun-Ju Lin, Yi-Sheng Lai, Shawn Chang, and Yu-Ting Huang, "ESD Performance Influence of a 60-V Lateral-diffused-MOST by the FOD Based (& Dotted-OD) Drain", [Lecture Notes in Electrical Engineering- Intelligent Technologies and Engineering Systems](#) (ISBN: 978-3-319-04572-6), vol. 293, Chap. 108, pp.883-890, New York, USA, Springer publisher, 2014.
9. Shen-Li Chen\*, Min-Hua Lee, Yi-Sheng Lai, Chun-Ju Lin, Yu-Ting Huang, and Shawn Chang, "Effect of Drain FODs on ESD/LU Immunities in the 60V High-voltage nLDMOS", [Lecture Notes in Electrical Engineering- Intelligent Technologies and Engineering Systems](#) (ISBN: 978-3-319-04572-6), vol. 293, Chap. 107, pp.875-882, New York, USA, Springer publisher, 2014.

### C. Referred Conference Papers: (2014~2023)

1. 楊修源, 陳勝利\*, 林廷恩, "高壓 nLDMOS 汲極端水平嵌入離散 P<sup>+</sup> SCR 之抗 ESD/栓鎖效應可靠度研究," [中國機械工程學會第四十屆全國學術研討會](#), Changhua, Taiwan, Dec. 2023, pp.927-929.
2. 林廷恩, 陳勝利\*, 楊修源, "高壓 nLDMOS 汲極端嵌入 STI 面積調變對可靠度增強之研究," [中國機械工程學會第四十屆全國學術研討會](#), Changhua, Taiwan, Dec. 2023, pp.930-932.
3. 陳勛祥, 林家丞, 陳勝利, "10 位元 10MHz 取樣頻率之 CMOS 導管式類比數位轉換器設計," [中國機械工程學會第四十屆全國學術研討會](#), Changhua, Taiwan, Dec.. 2023, pp.933-935.
4. 林廷恩, 陳勝利\*, 劉誌瑋, 楊修源, "高壓 nLDMOS 汲極端寄生 Schottky/SCR 面積調變之抗 ESD 能力探討," [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2023,

pp.C3-1- C3-4.

5. Xiu-Yuan Yang, Shen-Li Chen\*, Ting-En Lin, "高壓 nLDMOS 汲極端垂直嵌入 SCR 暨離散 P<sup>+</sup> SCR 之抗 ESD 能力研究," [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2023, pp.C2-1- C2-4.
6. Xiu-Yuan Yang, Shen-Li Chen\*, Ting-En Lin, "ESD-Robustness Study of High-voltage nLDMOSs with Vertically Embedded SCR and Discrete P<sup>+</sup> SCR in the Drain Side," [IEEE 5th Eurasia Conference on IoT, Communication and Engineering \(ECICE\)](#), Oct. 2023, pp.193-196.
7. Ting-En Lin, Shen-Li Chen\*, Zhi-Wei Liu, Xiu-Yuan Yang, "Impacts of Embedded SCR/Schottky Parasitics on ESD Reliability in the Drain Side of High Voltage nLDMOS Devices," [IEEE 5th Eurasia Conference on IoT, Communication and Engineering \(ECICE\)](#), Oct. 2023, pp.208-211.
8. Shen-Li Chen\*, Wei-Jung Chen, Chih-Ying Yen, "Analyzing ESD Reliability Strengthening of 40-V nLDMOS with Drain-Side Parasitic SCRs," [1616th International Conference on Recent Innovations in Engineering and Technology \(1616th ICRIET\)](#), Zurich, Switzerland, Aug. 2023, pp. 39-44.
9. Xiu-Yuan Yang, Shen-Li Chen\*, Jhong-Yi Lai, Xing-Chen Mai, Yu-Jie Chung, and Ting-En Lin, "ESD-capability Study of High-voltage nLDMOSs with the Drift Region DPW Engineering," [IEEE International Conference on Consumer Electronics \(ICCE-TW\)](#), Pingtung, Taiwan, Jul. 2023, pp.223-224.
10. Ting-En Lin, Shen-Li Chen\*, Zhi-Wei Liu, Xing-Chen Mai, Xiu-Yuan Yang, and Yu-Jie Chung, "High-voltage nLDMOS Drain Side Schottky/SCR Modulations for Enhancement Reliability Capabilities," [IEEE International Conference on Consumer Electronics \(ICCE-TW\)](#), Pingtung, Taiwan, Jul. 2023, pp.225-226.
11. Xing-Chen Mai, Shen-Li Chen\*, Jhong-Yi Lai, Zhi-Wei Liu, and Yu-Jie Chung, "ESD-capability Impacts of the Resurf NBL Length on High-voltage nLDMOSs," [9th IEEE International Conference on Applied System Innovation \(ICASI\)](#), Tokyo, Japan, Apr. 2023, pp.65-67.
12. Yu-Jie Chung, Shen-Li Chen\*, Xing-Chen Mai, Ting-En Lin, and Xiu-Yuan Yang, "Robust ESD Capability of High-voltage nLDMOSs with Embedded Floating P<sup>+</sup> Structures in the Drain Side," [9th IEEE International Conference on Applied System Innovation \(ICASI\)](#), Tokyo, Japan, Apr. 2023, pp.74-76.
13. Jhong-Yi Lai, Wei-Jung Chen, Shen-Li Chen\*, "Enhanced ESD-capability of High-voltage 32 V N-Channel LDMOSs with the Body-side Hetero-junction Structure," [13th International Conference on Power, Energy and Electrical Engineering](#), Tokyo, Japan, Feb. 2023, pp.17-21.
14. 鍾宇傑, 陳勝利\*, 麥新承, 林廷恩, 楊修源, "汲極端寄生蕭特基二極體/加入 STI 結構對高壓 nLDMOS 抗 ESD 能力之探討," [第十九屆台灣電力電子研討會](#), Taichung, Taiwan, Dec. 2022, pp.004-1- 004-4.
15. 麥新承, 陳勝利\*, 鍾宇傑, 楊修源, 林廷恩, "高壓 nLDMOS 在汲極側漂移區設計不同 RESURF 結構之抗 ESD 能力影響研究," [第十九屆台灣電力電子研討會](#), Taichung, Taiwan, Dec. 2022, pp.002-1- 002-4.
16. Yu-Jie Chung, Shen-Li Chen\*, Zhi-Wei Liu, Jhong-Yi Lai and Xing-Chen Mai, "汲極



端寄生蕭特基元件/矽控整流器並嵌入 HVPB 結構對高壓 nLDMOS 抗 ESD 能力影響之探討", [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2022, pp.B1-1- B1-5.

17. Xing-chen Mai, [Shen-Li Chen\\*](#), Yu-Jie Chung, Xiu-Yuan Yang and Ting-En Lin, "高壓 nLDMOS 三電極區寄生蕭特基二極體之 ESD 可靠度能力探討", [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2022, pp.B2-1- B2-6.
18. Xing-Chen Mai, [Shen-Li Chen\\*](#), Xiu-Yuan Yang, Ting-En Lin, and Yu-Jie Chung, " ESD-immunity Impacts of High-voltage nLDMOS with RESURF Structures in the Drain-side Drift Region", [International Conference on Machining, Materials and Mechanical Technologies \(IC3MT\)](#), Taipei, Taiwan, Nov. 2022. (accepted)
19. Yu-Jie Chung, [Shen-Li Chen\\*](#), Xing-Chen Mai, Xiu-Yuan Yang, and Ting-En Lin, "Robust ESD Ability of High Voltage nLDMOSs with Drain-side Adding Schottky/STI", [International Conference on Machining, Materials and Mechanical Technologies \(IC3MT\)](#), Taipei, Taiwan, Nov. 2022. (accepted)
20. Xing-Chen Mai , [Shen-Li Chen\\*](#), Yu-Jie Chung, Xiu-Yuan Yang, and Ting-En Lin, "Study of the Turns Impact on ESD-immunity of High-voltage nLDMOSs with a Constant Floating-poly Area", [IEEE 4th International Conference of Eurasia Conference on IOT, Communication and Engineering \(ECICE\)](#), Yunlin, Taiwan, Oct. 2022, pp.176-178.
21. Yu-Jie Chung, [Shen-Li Chen\\*](#), Zhi-Wei Liu, Jhong-Yi Lai and Xing-Chen Mai, " ESD-ability Analysis of High Voltage nLDMOSs with the Drain-side Parasitic Schottky/Embedded Shallow-trench Isolation", [IEEE 4th International Conference of Eurasia Conference on IOT, Communication and Engineering \(ECICE\)](#), Yunlin, Taiwan, Oct. 2022, pp. 151-153.
22. Hsun-Hsiang Chen, You Zhang, [Shen-Li Chen](#), "A Study of ESD Reliability on Gate and Drain to Source and Substrate Stress by Structure Modulation in 0.18  $\mu\text{m}$  6 V nLDMOS Devices", [IET International Conference on Engineering Technologies and Applications \(IET ICETA\)](#), Changhua, Taiwan, Oct. 2022, pp. 1-2.
23. Xing-Chen Mai, [Shen-Li Chen\\*](#), Jhong-Yi Lai, Zhi-Wei Liu, and Yu-Jie Chung, " ESD-immunity Study of High-voltage nLDMOS with Vertical Parasitic Schottky Structures in the Source End," [IET International Conference on Engineering Technologies and Applications \(IET ICETA\)](#), Changhua, Taiwan, Oct. 2022, pp. 1-2.
24. Yu-Jie Chung, [Shen-Li Chen\\*](#), Zhi-Wei Liu, Jhong-Yi Lai, and Xing-Chen Mai, " ESD-ability Enhancement of High Voltage pLDMOSs with the Discrete Source Side," [IET International Conference on Engineering Technologies and Applications \(IET ICETA\)](#), Changhua, Taiwan, Oct. 2022, pp. 1-2.
25. Xing-Chen Mai, [Shen-Li Chen\\*](#), Jhong-Yi Lai, Zhi-Wei Liu, and Yu-Jie Chung, " ESD-robustness Enhancement of High-voltage Octagonal nLDMOSs with an Embedded Schottky Diode Modulation in the Bulk Electrode," [The 5th NIT-NUU Bilateral Academic Conference](#), Miaoli, Taiwan, Sep. 5, 2022, pp.1-2.
26. Yu-Jie Chung, [Shen-Li Chen\\*](#), Zhi-Wei Liu, Jhong-Yi Lai, and Xing-Chen Mai, " Robust ESD Capability Design of High Voltage nLDMOSs with the Drain-side Parasitic SCR Structures by TCAD Simulation," [The 5th NIT-NUU Bilateral Academic Conference](#), Miaoli, Taiwan, Sep. 5, 2022, pp.1-2.

27. Zhi-Wei Liu, Shen-Li Chen\*, Jhong-Yi Lai, Xing-Chen Mai, and Yu-Jie Chung, "An Investigation of ESD-Enhancement by the Drain-side Embedded SCR Area Modulation for HV pLDMOSs," [IEEE International Conference on Consumer Electronics \(ICCE-TW\)](#), Taipei, Taiwan, Jul. 2022, pp.73-74.
28. Jhong-Yi Lai, Shen-Li Chen\*, Zhi-Wei Liu, Xing-Chen Mai and Yu-Jie Chung, "ESD Capability Analysis of High-voltage nLDMOSs by the Bulk Terminal Modulation," [IEEE International Conference on Consumer Electronics \(ICCE-TW\)](#), Taipei, Taiwan, Jul. 2022, pp. 71-72.
29. Shen-Li Chen\* and Po-Lin Lin, "Holding-voltage Enhancement of Power Management Silicon Based UHV 300-V Circular LDMOS Components by Source Side Engineering," [Advances in Functional Materials \(AFM\) Conference](#), Kyushu, Japan, July 2022. (accepted)
30. 鍾宇傑, 陳勝利\*, 劉誌瑋, 賴忠義, 麥新承, "汲極端寄生矽控整流器結構對高壓 nLDMOS 抗 ESD 能力探討," [第十六屆智慧生活科技研討會\(ILT2022\)](#), Taichung, Taiwan, Jun 2022, pp.239-242.
31. 麥新承, 陳勝利\*, 劉誌瑋, 賴忠義, 鍾宇傑, "汲極端寄生蕭特基二極體結構調變對於高壓 LDMOS 抗 ESD 能力之探討," [第十六屆智慧生活科技研討會\(ILT2022\)](#), Taichung, Taiwan, Jun 2022, pp.229-232.
32. Zhi-Wei Liu, Shen-Li Chen\* and Jhong-Yi Lai, "ESD Study of HV 65V nLDMOSs with the Drain-side Parasitic SCR Modulation," [International Electrostatic Discharge Virtual Workshop\(IEW\)](#), Hsinchu, Taiwan, May 3-6, 2022, pp.1-6.
33. Jhong-Yi Lai, Shen-Li Chen\* and Zhi-Wei Liu, "An ESD Investigation of 100V UHV nLDMOSs Embedded with the Schottky/SCR in the Drain End," [International Electrostatic Discharge Virtual Workshop\(IEW\)](#), Hsinchu, Taiwan, May 3-6, 2022, pp.1-6.
34. Shen-Li Chen\*, Shi-Zhe Hong and Wei-Jung Chen, "Robust HV Power pLDMOS Components for ESD Protection by the Drain-side Parasitic Schottky Diode and SCR Engineering," [International Power Electronics Conference \(IPEC-Himeji ECCE Asia\)](#), Himeji, Japan, May 2022, pp.1152-1156.
35. Jhong-Yi Lai, Shen-Li Chen\*, Zhi-Wei Liu, Xing-Chen Mai and Yu-Jie Chung, "An ESD Investigation of 100V UHV nLDMOSs Embedded with Schottky/SCR Components in the Drain Side," [The 8th IEEE International Conference on Applied System Innovation \(ICASI\)](#), Nantou, Taiwan, Apr. 2022, pp.50-53.
36. Zhi-Wei Liu, Shen-Li Chen\*, Jhong-Yi Lai, Yu-Jie Chung, and Xing-Chen Mai, "HV 65V nLDMOSs Engineering of ESD Enhancement by the Drain Side with Parasitic SCR Modulations," [The 8th IEEE International Conference on Applied System Innovation \(ICASI\)](#), Nantou, Taiwan, Apr. 2022, pp.46-49
37. Zhi-Wei Liu, Shen-Li Chen\*, Jhong-Yi Lai, Xing-chen Mai, Yu-Jie Chung, "Enhance the ESD Reliability of HV pLDMOS Transistors with the Embedded Horizontal SCR and Schottky Diode Techniques," [The 5th IEEE International Future Energy Electronics Conference](#), Taipei, Taiwan, Nov. 2021, pp.1-6.
38. Jhong-Yi Lai, Shen-Li Chen\*, Zhi-Wei Liu, Yu-Jie Chung, Xing-chen Mai, "ESD-capability Improvement of Ultra-high Voltage nLDMOS Components by the

Drain Side Engineering," [The 5th IEEE International Future Energy Electronics Conference](#), Taipei, Taiwan, Nov. 2021, pp.1-6.

39. 賴忠義、陳勝利\*、林柏霖、劉誌瑋、麥新承, "超高壓 nLDMOS 操作電壓調整對 ESD 可靠度能力探討," [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2021, pp.C2-1- C2-5.
40. Zhi-Wei Liu, Shen-Li Chen\*, Jhong-Yi Lai, Xing-Chen Mai, "圓形超高壓 nLDMOS 同心圓式 Poly 2 與漂移區超接面離散調變對抗 ESD 能力之影響," [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2021, pp.C1-1- C1-4.
41. Xing-Chen Mai, Shen-Li Chen\*, Shi-Zhe Hong , Jhong-Yi Lai, Zhi-Wei Liu and Yu-Jie Chung, "Study on the ESD Immunity of High-voltage pLDMOS with the Vertical Parasitic Schottky/SCR Structures in the Drain Electrode," [8th IEEE & 9th The International Conference on Science, Education, and Viable Engineering \(ICSEVEN 2021\)](#), Taitung, Taiwan, Oct. 2021.
42. Jhong-Yi Lai, Shen-Li Chen\*, Zhi-Wei Liu, Yu-Jie Chung and Xing-Chen Mai, " Research on ESD Reliability of Ultra-high Voltage nLDMOSs Modulated by Different Operating Voltages," [8th IEEE & 9th The International Conference on Science, Education, and Viable Engineering \(ICSEVEN 2021\)](#), Taitung, Taiwan, Oct. 2021.
43. Zhi-Wei Liu, Shen-Li Chen\*, Jhong-Yi Lai, Xing-Chen Mai and Yu-Jie Chung, "ESD Study of the Concentric Poly2 with Different Potentials and the Discrete HVPW Modulation on Circular Ultra-high Voltage nLDMOS Devices," [8th IEEE & 9th The International Conference on Science, Education, and Viable Engineering \(ICSEVEN 2021\)](#), Taitung, Taiwan, Oct. 2021.
44. Zhi-Wei Liu, Shen-Li Chen\*, Sheng-Kai Fan, Shi-Zhe Hong, Tien-Yu Lan, Yu-Jie Zhou and Jhong-Yi Lai, "ESD-capability Improvement of the Embedded Horizontal SCR Modulation for HV pLDMOS Devices," [The 4th NIT-NUU Bilateral Academic Conference](#), Miaoli, Taiwan, Sep. 2021, pp. 1-1.
45. Jhong-Yi Lai, Shen-Li Chen\*, Tien-Yu Lan, Yu-Jie Zhou, Shi-Zhe Hong and Zhi-Wei Liu, "ESD Protection Study of Ultra-high Voltage nLDMOS Device's Applications," [The 4th NIT-NUU Bilateral Academic Conference](#), Miaoli, Taiwan, Sep. 2021, pp. 1-1.
46. Yu-Jie Zhou, Shen-Li Chen\*, Tien-Yu Lan, Shi-Zhe Hong, Zhi-Wei Liu and Zhong-Yi Lai, " Improved UHV IGBT–Cell for ESD Protection with High Holding Voltage via a 0.5 $\mu$ m BCD Process," [IEEE International Conference on Consumer Electronics \(ICCE-TW\)](#), Penghu, Taiwan, Sep. 2021, pp. 1-2.
47. Shi-Zhe Hong, Shen-Li Chen\*, Tien-Yu Lan, Yu-Jie Zhou, Zhi-Wei Liu, and Jhong-Yi Lai, "ESD-Immunity Impact of HV pLDMOS with Drain-side Embedded Horizontal P-type Schottky Modulations," [IEEE International Conference on Consumer Electronics \(ICCE-TW\)](#), Penghu, Taiwan, Sep. 2021, pp. 1-2.
48. Tien-Yu Lan, Shen-Li Chen\*, Yu-Jie Zhou, Shi-Zhe Hong, Chung-Yi Lai, Zhi-Wei Liu, "Holding-voltage Improvement of UHV Circular nLDMOS Transistors by the Drain-side SCR Engineering," [IEEE International Conference on Consumer Electronics \(ICCE-TW\)](#), Penghu, Taiwan, Sep. 2021, pp. 1-2.
49. 劉誌瑋, 陳勝利\*, 范盛凱, 洪士哲, 藍天興, 周昱杰, 賴忠義, "車用 HV pLDMOS 元件汲

極內建水平 SCR 調變對 ESD 能力探討," 第一屆台灣智慧電動車及綠能科技研討會, 台灣台中, Jul.23, 2021, pp.E05-1-E05-4.

50. 賴忠義, 陳勝利\*, 藍天興, 周昱杰, 洪士哲, 劉誌瑋, "綠能用超高壓 nLDMOS 元件汲極端工程之靜電放電防護能力提升探討," 第一屆台灣智慧電動車及綠能科技研討會, 台灣台中, Jul.23, 2021, pp. E11-1- E11-3.
51. Yu-jie Zhou, Shen Li Chen, Tien-Yu Lan, Shi-Zhe Hong, Zhong-Yi Lai and Liu Zhi-Wei, "ESD Reliability Design of IGBT Cells with Parasitic Schottky Diodes in the Drain Side," [7th IEEE & 8th The International Conference on Science, Education, and Viable Engineering \(ICSEVEN 2021\)](#), Kinmen, Taiwan, Apr. 2021.
52. Shi-Zhe Hong, Shen-Li Chen, Tien-Yu Lan, Yu-Jie Zhou, Zhi-Wei Liu, and Jhong-Yi Lai, "ESD-Robustness Study of HV nLDMOS with Drain-side Embedded Parasitic Schottky/SCR Device Modulations," [7th IEEE & 8th The International Conference on Science, Education, and Viable Engineering \(ICSEVEN 2021\)](#), Kinmen, Taiwan, Apr. 2021.
53. Tien-Yu Lan, Shen-Li Chen\*, Yu-Jie Zhou, Shi-Zhe Hong, Chung-Yi Lai, Zhi-Wei Liu, "ESD-ability Investigation of the Elliptical UHV nLDMOS Transistors by the Different Types SCR in the Drain Side," [7th IEEE & 8th The International Conference on Science, Education, and Viable Engineering \(ICSEVEN 2021\)](#), Kinmen, Taiwan, Apr. 2021.
54. Yu-Jie Zhou, Shen-Li Chen\*, Tien-Yu Lan, Shi-Zhe Hong, Liu Zhi-Wei and Zhong-Yi Lai, "ESD Reliability Design of IGBT Cells with Parasitic Schottky Diodes in the Drain Side," [IEEE 7th The International Conference on Science, Education, and Viable Engineering \(ICSEVEN 2020\)](#), Penghu, Taiwan, Nov. 2020.
55. Shi-Zhe Hong, Shen-Li Chen\*, Sheng-Kai Fan, Tien-Yu Lan, Yu-Jie Zhou, Jhong-Yi Lai and Zhi-Wei Liu, "New Methods to Improve ESD Immunity on HV pLDMOS Devices with Drain-side Embedded Horizontal SCR Modulations," [IEEE 7th The International Conference on Science, Education, and Viable Engineering \(ICSEVEN 2020\)](#), Penghu, Taiwan, Nov. 2020.
56. Tien-Yu Lan, Shen-Li Chen\*, Yu-Jie Zhou, Shi-Zhe Hong, Zhi-Wei Liu and Jhong-Yi Lai, "SH\_P Ring and Concentration Gradient for ESD Enhancement in UHV Circular nLDMOS Transistors," [IEEE 7th The International Conference on Science, Education, and Viable Engineering \(ICSEVEN 2020\)](#), Penghu, Taiwan, Nov. 2020.
57. Po-Lin Lin, Shen-Li Chen\*, Sheng-Kai Fan, Tien-Yu Lan, Yu-Jie Zhou and Shi-Zhe Hong, "Improving the ESD Robustness of an Ultra-high voltage nLDMOS Device with the Embedded Schottky Diode," [IEEE International Conference on Consumer Electronics \(ICCE-TW\)](#), Taoyuan, Taiwan, Sep. 2020,pp. 1-2.
58. Sheng-Kai Fan, Shen-Li Chen\*, Po-Lin Lin, Shi-Zhe Hong, Tien-Yu Lan and Yu-Jie Zhou, "A Novel SCR-based Schottky Diode and Lightly P-well Additions of HV 60V nLDMOS on ESD Capability," [IEEE International Conference on Consumer Electronics \(ICCE-TW\)](#), Taoyuan, Taiwan, Sep. 2020,pp. 1-2.
59. Tien-Yu Lan, Shen-Li Chen\*, Hung-Wei Chen, Sheng-Kai Fan, Po-Lin Lin, Yu-Jie Zhou and Shi-Zhe Hong, "ESD-capability Influences of UHV Circular nLDMOS Transistors by the Drain-side Ladder-Step STI," [IEEE International Conference on](#)

[Consumer Electronics \(ICCE-TW\)](#), Taoyuan, Taiwan, Sep. 2020, pp. 1-2.

60. Tien-Yu Lan, [Shen-Li Chen\\*](#), Po-Lin Lin, Sheng-Kai Fan, Yu-Jie Zhou, Shi-Zhe Hong and Hung-Wei Chen, "ESD-ability Design of UHV Circular nLDMOS Transistors by the Super-junction Length's Modulation and Concentration Gradient," [3rd IEEE International Conference on Knowledge Innovation and Invention \(ICKII\)](#), Kaohsiung, Taiwan, Aug. 2020, pp. 78-79.
61. Yu-Jie Zhou, [Shen-Li Chen\\*](#), Pei-Lin Wu, Po-Lin Lin, Sheng-Kai Fan, Tien-Yu Lan, Shi-Zhe Hong, "ESD-capability Enhancement of Ultra-high Voltage nLDMOSs by the DPW Discrete Layer," [3rd IEEE International Conference on Knowledge Innovation and Invention \(ICKII\)](#), Kaohsiung, Taiwan, Aug. 2020, pp. 59-60.
62. Shi-Zhe Hong, [Shen-Li Chen\\*](#), Sheng-Kai Fan, Po-Lin Lin, Tien-Yu Lan, and Yu-Jie Zhou, "Strengthening the ESD Reliability of HV nLDMOSs with Drain-side Embedded Horizontal-type Schottky Devices," [3rd IEEE International Conference on Knowledge Innovation and Invention \(ICKII\)](#), Kaohsiung, Taiwan, Aug. 2020, pp. 57-58.
63. 洪士哲, [陳勝利\\*](#), 范盛凱, 林柏霖, 藍天興, 周昱杰, "電力轉換系統中之高壓 LDMOS ESD 可靠度強化研究," [全國系統科學與工程會議 \(National Symposium on Systems Science and Engineering\)](#), Taichung, Taiwan, June 2020, pp.1081-1-1081-1.
64. 藍天興, [陳勝利\\*](#), 林柏霖, 范盛凱, 周昱杰, 洪士哲, "電力系統用之超高壓 300V nLDMOS 汲極端工程對 ESD 能力影響," [全國系統科學與工程會議 \(National Symposium on Systems Science and Engineering\)](#), Taichung, Taiwan, June 2020, pp.1082-1-1082-1.
65. Po-Lin Lin, [Shen-Li Chen\\*](#), "Promote the ESD Reliability on 300-V Ultra-high Voltage nLDMOS Devices with the Novel Embedded Schottky Diode," [27th Symposium on Nano Device Technology](#), Hsinchu, Taiwan, May 2020, pp. CC00057-1-CC00057-1.
66. Sheng-Kai Fan, [Shen-Li Chen\\*](#), "Impacts of ESD Reliability on HV 60-V pLDMOS Devices by the Embedded SCR and Heterojunction Diode," [27th Symposium on Nano Device Technology](#), Hsinchu, Taiwan, May 2020, pp. CC00062-1-CC00062-1.
67. [Shen-Li Chen\\*](#), Sheng-Kai Fan, Po-Lin Lin, Shi-Zhe Hong, Tien-Yu Lan and Yu-Jie Zhou, "利用汲極寄生接面元件提升高壓 LDMOS 之抗 ESD 可靠度能力", [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2019, pp. B3-1 - B3-4.
68. [Shen-Li Chen\\*](#), Po-Lin Lin, Sheng-Kai Fan, Yu-Jie Zhou, Tien-Yu Lan and Shi-Zhe Hong, "超高壓 LDMOS 汲極端漂移區調變與寄生蕭特基二極體之抗 ESD 能力探討", [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2019, pp. B2-1 - B2-4.
69. Po-Lin Lin, [Shen-Li Chen\\*](#), Pei-Lin Wu, Yu-Lin Jhou and Sheng-Kai Fan, "Evaluating the Drift-region Length Effect of nLDMOS on ESD Ability with a TLP Testing System," [IEEE 8th Global Conference on Consumer Electronics \(GCCE\)](#), Osaka, Japan, Oct. 2019, pp.83-84.
70. Sheng Kai Fan, [Shen-Li Chen\\*](#), Yu-Lin Jhou, Pei-Lin Wu, and Po-Lin Lin, "ESD Immunity Impacts of the Drain-side Heterojunction Device Addition in HV 60 V n/pLDMOS Devices," [IEEE 8th Global Conference on Consumer Electronics \(GCCE\)](#),



Osaka, Japan, Oct. 2019, pp.81-82.

71. Sheng-Kai Fan, Shen-Li Chen\*, Po-Lin Lin, Shi-Zhe Hong, Tien-Yu Lan and Yu-Jie Zhou, "The Impact of Drift-region Length Reduction of n/pLDMOS on ESD Ability by TLP Measurements," [IEEE Eurasia Conference on IOT, Communication and Engineering](#), Yunlin, Taiwan, Oct. 2019, pp.199-120.
72. Po-Lin Lin, Shen-Li Chen\*, Sheng-Kai Fan, Yu-Jie Zhou, Tien-Yu Lan and Shi-Zhe Hong, "ESD-Immunity Influence of Ultra-high Voltage nLDMOS as the Drift Region Embedded a P-well," [IEEE Eurasia Conference on IOT, Communication and Engineering](#), Yunlin, Taiwan, Oct. 2019, pp.411-412.
73. 陳勝利\*, 周裕琳, 吳沛霖, 范盛凱, 林柏霖, 洪士哲, 藍天興, 周昱杰, "高壓 60V n/pLDMOS 汲極端異質接面對 ESD 靜電防護能力之影響," [第十六屆台灣電力電子研討會](#), Kaohsiung, Taiwan, Sep. 2019, pp. PE-013-94-1 - PE-013-94-5.
74. 陳勝利\*, 吳沛霖, 周裕琳, 林柏霖, 范盛凱, 周昱杰, 藍天興, 洪士哲, "圓形 300V nLDMOS 源極端/體極端接觸窗離散工程之抗 ESD 能力探討," [第十六屆台灣電力電子研討會](#), Kaohsiung, Taiwan, Sep. 2019, pp. PE-013-92-1 - PE-013-92-5.
75. Shen-Li Chen\*, Yu-Lin Jhou, Sheng-Kai Fan, Po-Lin Lin, "Effect of High-voltage nLDMOS in the Drain-side with Parasitic Schottky Diode and N<sup>+</sup> Area Modulation on ESD Capability," [International Conference On Electrical and Electronics Engineering\(ICEEE\)](#), Zurich, Switzerland, Aug. 2019, pp.1-4.
76. Shen-Li Chen\*, Pei-Lin Wu, Yu-Lin Jhou, Po-Lin Lin and Sheng Kai Fan, "ESD-Protection Design of UHV Circular nLDMOSs by the Drift Region with Elliptical Cylinder Super-junctions," [International Conference of advanced Technology Innovation](#), Sapporo, Japan, Jul. 2019. (accepted & Honorable Mentions winner)
77. Sheng Kai Fan, Shen-Li Chen\*, Yu-Lin Jhou, Pei-Lin Wu, and Po-Lin Lin, "Channel- & Drift Region's STI-Lengths Impacts of ESD Immunity in HV 60 V nLDMOS Devices," [IEEE International Conference on Consumer Electronics \(ICCE\)](#), Yilan, Taiwan, May 2019, pp.1-2.
78. Po-Lin Lin, Shen-Li Chen\*, Pei-Lin Wu, Yu-Lin Jhou and Sheng-Kai Fan, "ESD-Reliability Investigation of an UHV Elliptical LDMOS-SCR by the Drain-Side Junction Replacement," [IEEE International Conference on Consumer Electronics \(ICCE\)](#), Yilan, Taiwan, May 2019, pp.1-2.
79. Shen-Li Chen\*, Pei-Lin Wu, Yu-Lin Jhou, Po-Lin Lin and Sheng Kai Fan, "Robust the ESD Reliability by Drain-side Super-junction for the UHV Circular nLDMOS," [IEEE International Conference on Advanced Manufacturing](#), Yunlin, Taiwan, Nov. 2018, pp. 142-143.
80. Shen-Li Chen\*, Yu-Lin Jhou, Pei-Lin Wu, Sheng-Kai Fan and Po-Lin Lin, "ESD-Immunity Influence of 60-V pLDMOS by the Floating Polysilicon on Drain-side STI," [IEEE International Conference on Advanced Manufacturing](#), Yunlin, Taiwan, Nov. 2018, pp. 318-319.
81. Shen-Li Chen\*, Yu-Lin Jhou, Pei-Lin Wu, Sheng-Kai Fan and Po-Lin Lin, "漂移區浮接多晶矽對高壓 pLDMOS ESD 能力影響之探討," [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2018, pp. C3-1- C3-5.
82. Shen-Li Chen\*, Pei-Lin Wu, Yu-Lin Jhou, Po-Lin Lin and Sheng Kai Fan, "圓形 300V

超高壓 nLDMOS 汲極端超接面之 ESD 可靠度強化," [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2018, pp. C2-1- C2-5

83. Shen-Li Chen\*, Yi-Hao Chiu, Yu-Lin Jhou, Pei-Lin Wu, Po-Lin Lin, Yu-Jen Chen, "ESD-Reliability Enhancement in a High-voltage 60 V Square-type pLDMOS by the Guard-Ring Engineering," [IEEE Asia-Pacific Microwave Conference](#), Kyoto, Japan, Nov. 2018, pp.785-787.
84. Yu-Jen Chen and Shen-Li Chen\*, "Electrostatic-Discharge Behaviour and Analysis of a Power Management IC," [IEEE International Workshop on Electromagnetics: Applications and Student Innovation Competition](#), Nagoya, Japan, Aug. 2018, pp.1-2.
85. Shen-Li Chen\*, Yi-Hao Chiu, Chih-Hung Yang, Chun-Ting Kuo, Yu-Lin Lin, Yi-Hao Chiu, Yi-Hao Chao, Jen-Hao Lo, Yu-Lin Jhou, Pei-Lin Wu, "NBL Layer Impacts on ESD Reliability for 60-V Power pLDMOS Transistors," [IEEE International Conference on Consumer Electronics – Taiwan](#), Taichung, Taiwan, May 2018, pp.1-2.
86. Shen-Li Chen\*, Yu-Lin Lin, Yi-Cih Wu, Yi-Hao Chao, Yi-Hao Chiu, Pei-Lin Wu, Yu-Lin Jhou, Chun-Ting Kuo, Jen-Hao Lo, "An Upgrade of ESD-Reliability in HV 60-V nLDMOS Devices by the Drain-Side Engineering," [IEEE International Symposium on Next-Generation Electronics](#), Taipei, Taiwan, May 2018, pp.1-2.
87. Shen-Li Chen\*, Yi-Hao Chao, Chih-Ying Yen, Jen-Hao Lo, Chun-Ting Kuo, Yu-Lin Lin, Yi-Hao Chiu, Pei-Lin Wu, Yu-Lin Jhou, "Design and Enhancement of ESD Reliability in Circular UHV 300-V nLDMOS Power Components," [IEEE International Power Electronics Conference \(IPEC-Niigata-ECCE Asia\)](#), Niigata Japan, May 2018, pp.1145-1148.
88. Shen-Li Chen\*, Yi-Hao Chiu, Chun-Ting Kuo, Yu-Lin Lin, Yi-Hao Chao, Jen-Hao Lo, Pei-Lin Wu, Yu-Lin Jhou, "高壓 60V 方形 pLDMOS 增強 ESD 可靠度能力之保護環工程," [第十六屆微電子技術發展與應用研討會](#), May 2018, pp. 45-48 (ISBN: 986055747-0).
89. Shen-Li Chen\*, Jen-Hao Lo, Yi-Hao Chao, Yu-Lin Lin, Yi-Hao Chiu, Chun-Ting Kuo, Yu-Lin Jhou, Pei-Lin Wu, "圓形超高壓 300V nLDMOS 之可靠度能力提升策略," [第十六屆微電子技術發展與應用研討會](#), May 2018, pp.49-52 (ISBN: 986055747-0).
90. Shen-Li Chen\*, Chih-Hung Yang, Yu-Lin Lin, Chun-Ting Kuo, Jen-Hao Lo, Yi-Hao Chiu, Yi-Hao Chao, Yu-Lin Jhou, Pei-Lin Wu, "汲極 SCR 工程對 60V 功率 nLDMOS 組件之抗 ESD 能力提升探討," [第 20 屆全國機構與機器設計學術研討會](#), Changhua, Taiwan, Nov. 2017, pp. B1-3-1-B1-3-7.
91. Shen-Li Chen\*, Chih-Hung Yang, Yi-Hao Chiu, Chun-Ting Kuo, Yu-Lin Lin, Yi-Hao Chao, Jen-Hao Lo, Yu-Lin Jhou, Pei-Lin Wu, "高壓 60V nLDMOS 增強 ESD 可靠度能力之源極端工程," [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2017, pp. A4-1-A4-6.
92. Shen-Li Chen\*, Chih-Ying Yen, Jen-Hao Lo, Yi-Hao Chao, Chun-Ting Kuo, Yu-Lin Lin, Yi-Hao Chiu, Pei-Lin Wu, Yu-Lin Jhou, "圓形超高壓-300V nLDMOS 特性及抗 ESD 能力探討," [T-ESD & Reliability Conference](#), Hsinchu, Taiwan, Nov. 2017, pp. A5-1-A5-5.
93. Shen-Li Chen\*, Yi-Cih Wu, Chih-Hung Yang, Chih-Ying Yen, Kuei-Jyun Chen,

Jia-Ming Lin, Yi-Hao Chiu, Yu-Lin Lin, Chun-Ting Kuo, Jen-Hao Lo, Yi-Hao Chao, Hung-Wei Chen, "Source-end Design and Failure Study for ESD Enhancement of 60 V nLDMOS Devices," [IEEE 24th International Symposium on the Physical and Failure Analysis of Integrated Circuits \(IPFA 2017\)](#), Chengdu, China, Jul. 2017, pp.1-4.

94. Shen-Li Chen\*, Chih-Hung Yang, Chih-Ying Yen, Kuei-Jyun Chen, Yi-Cih Wu, Jia-Ming Lin, Chun-Ting Kuo, Yu-Lin Lin, Yi-Hao Chiu, Yi-Hao Chao, Jen-Hao Lo, Hung-Wei Chen, "Novel Parasitic-SCR Impacts on ESD Robustness in the 60 V Power pLDMOS Devices," [International Conference on Consumer Electronics – Taiwan](#), Taipei, Jun. 2017, pp. 381-382.
95. Shen-Li Chen\*, Chih-Hung Yang, Kuei-Jyun Chen, Yi-Cih Wu, Yu-Lin Lin, Yi-Hao Chiu, Chun-Ting Kuo, Chih-Ying Yen, Jia-Ming Lin, Yi-Hao Chao, Jen-Hao Lo, "ESD-Improvement Comparisons of HV n-/p-LDMOS Components by the Bulk Modulations," [IEEE International Future Energy Electronics Conference- ECCE Asia](#), Kaohsiung City, Taiwan, Jun. 2017, pp. 2182-2186.
96. Yu-Jen Chen, Shen-Li Chen\*, Min-Hua Lee, "ESD-Reliability Influence on LV/HV MOSFET Devices by Different Zapping-voltage Steps in the Transmission-Line Pulse Testing," [IEEE International Conference on Applied System Innovation](#), Sapporo, Japan, May 2017, pp.1407-1410.
97. Shen-Li Chen\*, Chih-Ying Yen, Chih-Hung Yang, Yi-Cih Wu, Kuei-Jyun Chen, Yu-Lin Lin, Yi-Hao Chiu, Yi-Hao Chao, Hung-Wei Chen, Dylan Chen, Marty Lo, Jia-Ming Lin, Chun-Ting Kuo, Jen-Hao Lo, "ESD-Immunity Evaluations of a 40 V nLDMOS with Embedded SCRs in the Drain Side," [IEEE International Symposium on Next-Generation Electronics](#), Keelung, Taiwan, May 2017, pp. 1-2.
98. Shen-Li Chen\*, Jia-Ming Lin, Chih-Ying Yen, Yi-Hao Chao, Jen-Hao Lo, Kuei-Jyun Chen, Chih-Hung Yang, Yi-Cih Wu, Yi-Hao Chiu, Yu-Lin Lin, Chun-Ting Kuo, "Channel Length, Drift-region Distance, and Unit-Finger Width Impacts on the HBM Robustness for the 600 V N-Channel LDMOS Transistors," [International Conference on Engineering and Advanced Technology](#), Hong Kong, Dec. 2016, pp. 198-203.
99. Shen-Li Chen\*, Chih-Ying Yen, Jia-Ming Lin, Jen-Hao Lo, Yi-Hao Chao, Yi-Cih Wu, Kuei-Jyun Chen, Chih-Hung Yang, Chun-Ting Kuo, Yi-Hao Chiu, Yu-Lin Lin, "HBM-Reliability Influences of Channel Length and Drift-region Modulations in the 600 V UHV N-channel LDMOS Devices," [International Electron Devices and Materials Symposium \(IEDMS-2016\)](#), Taipei City, Taiwan, Nov. 2016, pp.19-1-19-2.
100. Shen-Li Chen\*, Yu-Ting Huang, Chih-Hung Yang, Kuei-Jyun Chen, Yi-Cih Wu, Jia-Ming Lin, Chih-Ying Yen, "ESD Reliability Improvement by the Source-Discrete Placement in a 45-V pLDMOS-SCR (nnp-Type)," [IEEE 6th International Conference on Power and Energy \(PECON\)](#), Melaka, Malaysia, Nov. 2016, pp. 68-71.
101. Shen-Li Chen\*, Yu-Ting Huang, Chih-Ying Yen, Kuei-Jyun Chen, Yi-Cih Wu, Jia-Ming Lin, and Chih-Hung Yang, "ESD Protection Structure Design for the 45-V pLDMOS-SCR (p-n-p-Arranged) Devices with Source-Discrete Distributions," [IEEE 5th Global Conference on Consumer Electronics \(GCCE\)](#), Kyoto, Japan, Oct. 2016,

pp. 1-2.

102. Shen-Li Chen\*, Yu-Ting Huang, Chih-Ying Yen, Kuei-Jyun Chen, Yi-Cih Wu, Jia-Ming Lin, and Chih-Hung Yang, "ESD Protection Structure Design with Source-Isolated Distributions for the pLDMOS on a 60-V Process," [5th International Multi-Conference on Engineering and Technology Innovation](#), Taichung, Taiwan, Oct. 2016. (accepted)
103. Shen-Li Chen\*, Min-Hua Lee, and Tzung-Shian Wu, "Influences of Substrate Pickup Integrated with the Source-end Engineering on ESD/Latch-up Reliabilities in a 0.35- $\mu$ m 3.3-V Process," [IEEE International Symposium on Computer, Consumer and Control](#), Xi'an, China, Jul. 2016, pp. 632 - 635.
104. Shen-Li Chen\*, Yi-Cih Wu, Jia-Ming Lin, Chih-Hung Yang, Chih-Ying Yen, Kuei-Jyun Chen, Hung-Wei Chen, "ESD Reliability Improvement of the 0.25- $\mu$ m 60-V Power nLDMOS with Discrete Embedded SCRs Separated by STI Structures," [IEEE 8th International Power Electronics and Motion Control Conference - ECCE Asia](#), Hefei, Anhui, China, May 2016, pp.1611-1614.
105. Shen-Li Chen\*, Yu-Ting Huang, Yi-Cih Wu, Jia-Ming Lin, Chih-Hung Yang, and Chih-Ying Yen, and Kuei-Jyun Chen,, "ESD-Reliability Characterizations of a 45-V p-Channel LDMOS-SCR with the Discrete-Cathode End," [IEEE International Conference on Applied System Innovation](#), Okinawa, Japan, May 2016, pp. 1-2.
106. Shen-Li Chen\*, Chih-Hung Yang, Chih-Ying Yen, Kuei-Jyun Chen, Yi-Cih Wu, and Jia-Ming Lin, "Design on ESD Robustness of Source-side Discrete Distribution in the 60-V High-Voltage nLDMOS Devices," [IEEE International Conference on Consumer Electronics](#)–Nantou, Taiwan, May 2016, pp.1-2.
107. Shen-Li Chen\*, Kuei-Jyun Chen, Yi-Cih Wu, Jia-Ming Lin, Chih-Hung Yang, and Chih-Ying Yen, "ESD Reliability Evaluations of the 60-V nLDMOS by the Drain-side Discrete SCRs," [IEEE International Symposium on Next-Generation Electronics](#), Hsinchu, Taiwan, May 2016, pp.1-2.
108. Shen-Li Chen\*, Kuei-Jyun Chen, Jia-Ming Lin, Chih-Hung Yang, Chih-Ying Yen, and Yi-Cih Wu, "Anti-ESD Study of nLDMOS with Drain-side Embedded SCR and Isolated STI Structures," [International Electron Devices and Materials Symposium \(IEDMS-2015\)](#), pp. B10-1 ~ B10-2, Kaohsiung City, Taiwan, Nov. 2015.
109. Shen-Li Chen\*, Kuei-Jyun Chen, Yi-Cih Wu, Jia-Ming Lin, Chih-Hung Yang, and Chih-Ying Yen, "nLDMOS 汲極端寄生 SCR 暨 STI 隔離調變之抗 ESD 能力探討," [T-ESD & Reliability Conference](#), pp. D3-1 ~ D3-5, Hsinchu, Taiwan, Nov. 2015.
110. Shen-Li Chen\*, Yi-Cih Wu, Jia-Ming Lin, Chih-Hung Yang, Chih-Ying Yen, and Kuei-Jyun Chen, "60-V nLDMOS 汲極端離散分佈式 SCR 之抗 ESD 可靠度分析," [T-ESD & Reliability Conference](#), pp. D4-1 ~ D4-5, Hsinchu, Taiwan, Nov. 2015.
111. Shen-Li Chen\*, Shawn Chang, Yu-Ting Huang, Chih-Ying Yen, Kuei-Jyun Chen, Yi-Cih Wu, Jia-Ming Lin, and Chih-Hung,Yang, "Impacts on the Anti-ESD/ Anti-LU Immunities by the Drain-side Superjunction Structure of HV/ LV nMOSFETs," [IEEE International Future Energy Electronics Conference](#), pp. 1-5, Taipei, Taiwan, Nov. 2015.
112. Shen-Li Chen\*, Yu-Ting Huang, "Drain Side Super Junctions Co-worked with

"nnpn" Arranged SCRs on ESD Robustness in the 60-V nLDMOS Devices," [International Technical Conference of IEEE Region 10 \(TENCON\)](#), pp. 1-4, Macau, China, Nov. 2015.

113. [Shen-Li Chen\\*](#), Yu-Ting Huang, Chih-Hung Yang, Chih-Ying Yen, Kuei-Jyun Chen, Yi-Cih Wu, and Jia-Ming Lin, "Drain Side N<sup>+</sup> Layout Manners ("nnpnpn" Arranged-type) on ESD Robustness in the 60-V pLDMOS-SCR", [12th International Symposium on Measurement Technology and Intelligent Instruments](#), Taipei, Taiwan, Sep. 2015. (accepted)
114. [Shen-Li Chen\\*](#), Dun-Ying Shu, "By Using Grey System and Neural-Fuzzy Network Methods to obtain the Threshold Voltage of Submicron n-MOSFET DUTs", [IEEE 12th International Conference on Fuzzy Systems and Knowledge Discovery \(FSKD\)](#), pp. 501-505, Zhangjiajie, China, Aug. 2015.
115. [Shen-Li Chen\\*](#), Yu-Ting Huang, "Drain-Side Discrete-Distributed Layout Influences on Reliability Issues in the 0.25  $\mu$ m 60-V Power pLDMOS", [9th IEEE International Conference on Power Electronics – ECCE Asia](#), pp. 581-587, Seoul, Korea, Jun. 2015.
116. [Shen-Li Chen\\*](#), Shawn Chang, Yu-Ting Huang, Shun-Bao Chang, "Anti-ESD Impacts on 60-V P-channel LDMOS Devices as None-ODs Zone Inserting in the Bulk Region", [IEEE International Conference on Consumer Electronics](#), pp. 266-267, Taipei, Taiwan, Jun. 2015.
117. [Shen-Li Chen\\*](#), Yu-Ting Huang, Shawn Chang, Shun-Bao Chang, "ESD Reliability Building in 0.25  $\mu$ m 60-V p-channel LDMOS DUTs with Different Embedded SCRs", [IEEE International Conference on Consumer Electronics](#), pp. 268-269, Taipei, Taiwan, Jun. 2015.
118. [Shen-Li Chen\\*](#), Chun-Ju Lin, Shawn Chang, Yu-Ting Huang, and Shun-Bao Chang, "ESD Reliability Comparison of Different Layout Topologies in the 0.25- $\mu$ m 60-V nLDMOS Power Devices", [IEEE International Symposium on Next-Generation Electronics](#), pp. T4-4-1- T4-4-4, Taipei, Taiwan, May 2015.
119. [Shen-Li Chen\\*](#), Yu-Ting Huang, Shawn Chang, and Shun-Bao Chang, "Influences of Drain Side P<sup>+</sup> Discrete-Islands on ESD Robustness in the 60-V pLDMOS-SCR ("PNPNP" Arranged-type)", [IEEE International Symposium on Next-Generation Electronics](#), pp. T4-5-1- T4-5-4, Taipei, Taiwan, May 2015.
120. [Shen-Li Chen\\*](#), Shawn Chang, Yu-Ting Huang, Shun-Bao Chang, "Reliability and Electrical Performance Influences by the Bulk-FOX Adding in 60-V pLDMOS Power Devices", [IEEE 10th International Green Energy Conference \(IGEC-X\)](#), pp. 1382-1-1382-4, Taichung, Taiwan, May 2015.
121. [Shen-Li Chen\\*](#), Yu-Ting Huang, Shawn Chang, Shun-Bao Chang, "Impacts of Drain-side "nnpn" Modulated-type SCRs on ESD Immunity in 60-V pLDMOS Power Components", [IEEE 10th International Green Energy Conference \(IGEC-X\)](#), pp. 1407-1-1407-4, Taichung, Taiwan, May 2015.
122. [Shen-Li Chen\\*](#) and Su-Ping Lee, "An Optimized Design of Performance Parameters for a 100V High-voltage N-channel LDMOS", [International Conference on Power Electronics and Energy Engineering \(PEEE\)](#), pp. 22-25, Phuket, Thailand,



Apr. 2015.

123. Shen-Li Chen\*, Chun-Ju Lin, Yu-Ting Huang, and Shawn Chang, "Layout Structure Dependence of 60-V nLDMOS DUTs in Reliability Considerations," [IEEE 3rd Global Conference on Consumer Electronics](#), Tokyo, Japan, Oct. 2014. (accepted)
124. Shen-Li Chen\*, Shawn Chang, Yu-Ting Huang, Shun-Bao Chang, "FOD Adding Dependences on 60-V pLDMOS Power DUTs in ESD Considerations," [International Forum on Systems and Mechatronics \(IFSM\)](#), Tainan, Taiwan, pp. E07-1 ~ E07-8, Oct. 2014.
125. Shen-Li Chen\*, Yu-Ting Huang, Shawn Chang, Shun-Bao Chang, "Layout-Type Influences of Anti-ESD Ability in 60-V pLDMOS Power DUTs with the Embedded SCR," [International Forum on Systems and Mechatronics \(IFSM\)](#), Tainan, Taiwan, pp. E16-1 ~ E16-9, Oct. 2014.
126. Shen-Li Chen\* and Chin-Chai Chen, "Photoluminescence Characteristic Enhancement of an n-GaN Blue LED material After a Dry Etching Process by Annealing Treatment", [6th International Symposium on Functional Materials \(ISFM\)](#), Singapore, pp. 190-193, Aug. 2014.
127. Shen-Li Chen\*, Min-Hua Lee, "TLP Characterization and Leakage-Biasing-Voltage ( $V_{LB}$ ) Correlations in MOSFET Measurements," [IEEE International Symposium on Computer, Consumer and Control](#), Taichung, Taiwan, pp. 199 ~ 202, Jun. 2014.
128. Shen-Li Chen\*, Chin-Chai Chen, "Annealing Treatment Influence on Photoluminescence of the n-GaN Blue LED After a Dry Etching Process," [IEEE International Symposium on Computer, Consumer and Control](#), Taichung, Taiwan, pp. 203 ~ 206, Jun. 2014.
129. Shen-Li Chen\*, Min-Hua Lee, "ESD Reliability Influence of a 60 V Power LDMOS by the FOD-Based (& Dotted-OD) Drain," [IEEE International Power Electronics Conference](#), Hiroshima, Japan, pp. 236 ~ 239, May 2014.
130. Shen-Li Chen\*, Min-Hua Lee, Chun-Ju Lin, Yi-Sheng Lai, Shawn Chang, Yu-Ting Huang, "Robust Design of HV pLDMOS-ESCR Structures in a 60-V BCD Process", [IEEE International Symposium on Next-Generation Electronics](#), Taoyuan, Taiwan, pp. Y1-11-1 ~ Y1-11-4, May 2014.
131. Shen-Li Chen\*, Min-Hua Lee, Yi-Sheng Lai, Chun-Ju Lin, Yu-Ting Huang, Shawn Chang, "Reliability Evaluation of the HV nLDMOS with Embedded Stripe-type SCR Structures", [IEEE International Symposium on Next-Generation Electronics](#), Taoyuan, Taiwan, pp. Y1-8-1 ~ Y1-8-4, May 2014.
132. Shen-Li Chen\*, Chun-Ju Lin, Yi-Sheng Lai, Yu-Ting Huang, and Shawn Chang, "ESD Robustness Evaluation in 60-V nLDMOS DUTs by Different Layout Types," [2014 Symposium on Nano Device Technology \(SNDT-2014\)](#), Hsinchu, Taiwan, pp. HF-12-1 ~ HF-12-4, May 2014.
133. Shen-Li Chen\*, Yi-Sheng Lai, Chun-Ju Lin, Shawn Chang, and Yu-Ting Huang, "A Study of ESD Robustness in the HV LDMOS with Super-Junction Structures," [2014 Symposium on Nano Device Technology \(SNDT-2014\)](#), Hsinchu, Taiwan, pp. HF-5-1 ~ HF-5-4, May 2014.

#### D. Patents 專利：(2014~2023)

1. 陳勝利, "具抗靜電放電及抗閃鎖能力之蕭特基接面場效電晶體", 中華民國新型專利, 證書 # TW M607285, pp. 9211-9220, 2021.02.01 ~ 2030.11.01.
2. 陳昱臻, 林吉聰, 陳勝利, "簡化型蕭特基能障穿隧塊材式場效電晶體", 中華民國新型專利, 證書 # TW M598528, pp. 12396-12401, 2020.07.11 ~ 2030.04.14.
3. 陳勝利, "具有矽控整流器結構之高壓半導體元件", 中華民國新型專利, 證書 # TW M518408, pp. 14213-14217, 2016.03.01 ~ 2025.09.23.
4. 陳勝利, "抗靜電放電的高壓半導體元件", 中華民國新型專利, TW M518409, pp. 14218-14220, 2016.03.01 ~ 2025.09.23.
5. 陳勝利, "抗靜電放電高壓半導體器件", 中華人民共和國實用新型專利, 證書 # CN 205303469 (ZL2015-2-1083639.7), pp. 1 ~ 9, (2015.12.23 ~ 2024.12.22).
6. 陳勝利, "具有可控硅結構之高壓半導體器件", 中華人民共和國實用新型專利, 證書 # CN 205303464 (ZL2015-2-1085705.4), pp. 1 ~ 11, (2015.12.23 ~ 2024.12.22).
7. 陳勝利, "高壓半導體器件", 中華人民共和國實用新型專利, 證書 # CN 4096403 (ZL2014-2-0484361.3), pp. 1 ~ 15, 2014.08.26 ~ 2023.08.25.
8. 陳勝利, "半導體結構", 中華人民共和國實用新型專利, 證書 # CN 4085412 (ZL2014-2-0375327.2), pp. 1 ~ 11, 2014.07.08 ~ 2023.07.07
9. 陳勝利, "發光二極管", 中華人民共和國實用新型專利, 證書 # CN 4050394 (ZL2014-2-0375246.2), pp. 1 ~ 11, 2014.07.08 ~ 2023.07.07
10. 陳勝利, "高壓半導體元件", 中華民國新型專利, 證書 # TW M488745, pp. 14915-14920, Oct. 2014, (2014.10.21 ~ 2024.07.14).
11. 陳勝利, "發光二極體", 中華民國新型專利, 證書 # TW M487526, pp. 16151-16157, Oct. 2014 (2014.10.01 ~ 2024.05.25).
12. 陳勝利, "具有高靜電放電防護能力的半導體結構", 中華民國新型專利, 證書 # TW M482841, pp. 14786-14788, Jul. 2014 (2014.07.21 ~ 2024.01.07).

#### E. Research Projects (研究計劃)：(2011~2023)

年度	補助類別	計畫名稱	擔任工作	執行期間
112	國科會專題研究計畫 (一般型研究計畫)	BCD 高壓製程之電源管理 IC 30-90V 輸出埠八邊型 LDMOS 組件強化抗 ESD/ Latch-up 可靠度能力提升研究 (NSTC 112-2221-E-239-004)	計畫主持人	112/08/01 ~ 113/07/31
111	科技部專題研究計畫 (一般型研究計畫)	電極內建蕭特基/SCR 架構可靠度設計之電源管理應用圓形超高壓功率 LDMOS 組件研究 (MOST 111-2221-E-239 -014)	計畫主持人	111/08/01 ~ 112/07/31
110	科技部專題研究計畫 (一般型研究計畫)	電源管理系統輸出級 200V~300V 橢圓超高壓功率 LDMOS 組件之抗 ESD 工程設計研究 (MOST 110-2221-E-239-013)	計畫主持人	110/08/01 ~ 111/07/31

109	科技部專題研究計畫 (一般型研究計畫)	高 ESD 防護能力設計之電源轉換應用 100V~300V 超高壓 nLDMOS 組件研究 (MOST 109-2221-E-239-015)	計劃主持人	109/08/01 ~ 110/07/31
108	科技部專題研究計畫 (一般型研究計畫)	電源管理應用上圓形超高壓功率 LDMOS 組件高可靠度設計研究 (MOST 108-2221-E-239-012)	計劃主持人	108/08/01 ~ 109/07/31
107/11~109/10	康舒科技股份有限公司	PWM 控制晶片設計所需的高壓靜電放電保護元件研究 (A107-1055)	計劃主持人	107/11~109/10
106	力晶科技公司	開發 ESD 防護元件在 55nm/40nm 高壓平台	計劃主持人	106/1~ 108/12
106	科技部專題研究計畫 (一般型研究計畫)	電力轉換超高壓 LDMOS 高抗靜電可靠度防護工程研究 (MOST 106-2221-E-239-018)	計劃主持人	106/08/01 ~ 107/07/31
105	科技部專題研究計畫 (一般型研究計畫)	電源管理功率積體電路輸出驅動埠電性與高可靠度能力提升研究 (MOST 105-2221-E-239-017)	計劃主持人	105/08/01 ~ 106/07/31
105	鉅晶科技公司	0.18um 6V_40V(6V_18V_60V) 功率製程 ESD 全晶片防護(元件)設計開發 (A105-1024)	計劃主持人	105/04~107/01
104	科技部專題研究計畫 (一般型研究計畫)	綠能組件電源埠防護佈局工程與抗 ESD 能力模型化研究 (MOST 104-2221-E-239-013)	計劃主持人	104/08/01 ~ 105/07/31
103	科技部專題研究計畫 (一般型研究計畫)	高壓製程電源管理組件之結構調變可靠度影響研究 (MOST 103-2221-E-239 -014)	計劃主持人	103/08/01 ~ 104/07/31
102	國科會專題研究計畫 (一般型研究計畫)	照明高壓驅動組件高可靠度佈局工程研究 (NSC 102-2221-E-239 -015)	計劃主持人	102/08/01 ~ 101/07/31
100	國科會專題研究計畫 (一般型研究計畫)	高可靠性低驟回之車用高壓 nLDMOS 元件研究 (NSC 100-2221-E-239 -003)	計劃主持人	100/08/01 ~ 101/07/31